[1] a) Simplify the following expression using ONLY the consensus theorem: (5 Marks)
   
   (i) \( W'Y'+WYZ+XY'Z+WX'Y \) (reduce to a sum of three product terms)

b) Simplify to a sum of three product terms (10 Marks)
   
   (i) \( F(A,B,C,D)=\Sigma m(0,2,4,6,8,10,12,14) \)

c) implement the function \( F \) using: (25 Marks)
   
   (i) 2-1 Mux (with \( A \) as the only select signal) (20 Marks)
   
   (ii) 4-16 DeMux (5 Marks)

[2] Write a single VHDL code to implement the following logic functions: (10 Marks)

\[
\begin{align*}
F(x,y,z,w) &= (x + y)' + (x + w)'(z + w) \\
H(x,y,z) &= (x + y)'z
\end{align*}
\]

Use separate signals for each of the operations in parentheses.

[3] In an Analog-to-Digital subsystem on a microcontroller, it is possible to control the sampling rate of the analog signal at the analog input port. A prescaler value is used to further divide the operating clock frequency (P Clock). The P clock goes through two different divider stages. The first divide factor is set by a binary value written to \( PRS[1:0] \). The effective frequency after stage one is the P clock divided by the factor \( 2^{(PRS[1:0] +1)} \). The second divider stage is always two. Build the above TWO STAGES of the frequency divider necessary for the proper operation of the A/D converter. Draw a complete state diagram and a state table for the circuit. Use JK flip-flops. (25 Marks)

[4] For the circuit shown in Figure 1, starting at \( Q_aQ_bQ_c = 000 \), assume an input sequence of 010110 is applied at X one at a time. Decide if the circuit in Figure 2 will ever sequence. If your answer is Yes, derive the state table for the above input sequence. (25 Marks)