Question one (25 Marks)
In VHDL, design a Finite State Machine FSM that samples a continuous stream of data on an input X. The FSM is to issue an output of 1 any time the sequence 1101 occurs. Consider that the sequence can be overlapping, for example:
X =…110110111…
Z = …000100100….  
(25 Marks)

Question Four: (15 Marks)
Choose the correct answer
i) The internal function of a block of hardware is:
   (a) design entity
   (b) architecture
   (c) package
   (d) signal

ii) In the following process, How many times does this process execute in response to an event on A:
   P1: process(A,B,D)
   begin
   B<=A after 5 NS;
   C<=B after 5 NS;
   D<=A and B after 5 NS;
   end process P1;
   (a) Not at all
   (b) Twice
   (c) Three times
   (d) Once only

iii) At what time the final wait statement execute?
   P2: process
   begin
   B<='0';
   wait for 20 NS;
   B<='1' after 10 NS;
   wait for 5 NS;
   C<=B after 1 NS;
   wait;
   end process;
   (a) 25 NS
   (b) 36 NS
   (c) 35 NS
   (d) None of the above

iv) The definition of the interface to a block of hardware is:
   (a) design entity
   (b) architecture
   (c) package
(d) entity

v) Look at the VHDL code below and decide what kind of hardware would be synthesized.

<table>
<thead>
<tr>
<th>Process</th>
<th>(a) None</th>
</tr>
</thead>
<tbody>
<tr>
<td>begin</td>
<td>(b) A transparent latch</td>
</tr>
<tr>
<td>if clock = ‘0’ then</td>
<td>(c) Multiplexer</td>
</tr>
<tr>
<td>F&lt;=‘0’;</td>
<td>(d) An and gate</td>
</tr>
<tr>
<td>else</td>
<td></td>
</tr>
<tr>
<td>F&lt;=A;</td>
<td></td>
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<tr>
<td>end if;</td>
<td></td>
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<tr>
<td>end process;</td>
<td></td>
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</tbody>
</table>

Question Three (60 Marks)

a) Starting from AND, OR and NOT gates only, design one-bit full adder VHDL representation (10 Marks)

b) Using the above design extend your design to a 4-bit adder/subtractor (12.5 Marks)

c) Create a four-bit adder/subtractor component and use it to create a eight-bit adder/subtractor (12.5 Marks)

d) Use the eight-bit adder to design a circuit performing a multiplication by addition in VHDL.