You are to design the data path and control of a RISC type 16-bit multi-cycle processor as indicated below:

- Eight 16-bit general-purpose registers (R₀ - R₇)
- Instruction set architecture:
  - add, sub, addi, subi, and, or, xor, slt, lw, sw, beq, jr, j

Your document should include the following:

2. A complete documented design of the ALU. This should be a paper design.
3. Detail design of datapath; your design should only use temporary registers if necessary. This should be a paper design.
4. Implementation of the control unit using a state machine. The state machine needs to be implemented using state editor of Xilinx or VHDL, and verified using Model SIM. Tutorials on these tools are available at http://www.engr.newpaltz.edu/~bai/CSE45208/cse45208.html
5. Detailed microprogramming implementation of the control unit. All needs to be specified including details of any dispatched ROM.

Due Date: December 6, 2004

Project guidelines:

Late projects are not accepted. If your project is not complete by the due date, you should hand in the incomplete project for a partial credit.

Project reports should professionally be documented and should consist of following.
You should use a word processor and a CAD tool to document your work.

Your report should be properly placed in a folder. The report should have the following sections:

- A departmental cover sheet indicating title of the project, course name and number, date (semester and year), and the name of each group member (up to 2 people per group are allowed).
- Table of contents.
- Introduction - describing the project for a practicing engineering.
- Procedure - your complete design including the circuitry. This may be broken into subsections. For example, a subsection can be devoted to the design of the ALU and another subsection to the design of datapath, etc.
- Conclusion (problems encountered, lessons learned, etc.).
- Your report needs to be free of grammatical and spelling errors.
- Your project should reflect your own work. If unreasonable similarities are recognized between the turned in projects, they will receive failing grades.