Question 1 (15 Points)
Do problem 5.3

Question 2 (15 Points)
Do problem 5.9

Question 3 (15 Points)
Do problem 5.13

Question 4 (15 Points)
Do problem 5.29

Question 5 (15 Points)
Do problem 5.30

Question 6 (15 Points)
Do problem 5.32

Question 7 (15 Points)
Assume the following operation times for the functional units of the architecture given in Figure 5.17. What is the minimum cycle time that you should use for this architecture?

- 6 nano second for the ALU
- 3 nano second for an adder
- 1 nano second for a multiplexer, a shifter or a sign extender
- 8 nano second for register read or write
- 10 nano second for a memory operation

Question 8 (15 Points)
We wish to add to the architecture of Figure 5.17 the capability of executing an instruction \( \text{js}\ Sr1, Sr2 \) Where $r1$ is encoded in "instruction[25-21]" and $r2$ is encoded in "instruction[20-16]" ("instruction[0-15]" are not used). The "js" instruction is a special subroutine call instruction. It causes PC+4 to be stored in $r1$ and it copies $r2$ into the PC. The result is a jump to the memory location whose address is in $r2$ while preserving the return address. Add any necessary datapaths and control signals to the architecture of Figure 5.17.

Question 9 (25 Points)
You are to redesign the multi-cycle processor specified in Figure 5.28 without the inclusion of registers A, B, and MDR.

a. Can this be done for the same instruction set i.e. lw, sw, R-type (add, sub, and, or, slt), beq, and j? If so, show the new datapath.

b. For part a, design the state diagram of the control unit.

c. Implement the control unit using the microprogramming.

Due November 9, 2005