Question 6 (15 Points)
Assume the following operation times for the functional units of the architecture given in Figure 5.17. What is the minimum cycle time that you should use for this architecture?

- 6 nano second for the ALU
- 3 nano second for an adder
- 1 nano second for a multiplexer, a shifter or a sign extender
- 8 nano second for register read or write
- 10 nano second for a memory operation

Question 7 (15 Points)
We wish to add to the architecture of Figure 5.17 the capability of executing an instruction \( \text{js} \ r1, r2 \) Where \( r1 \) is encoded in "instruction[25-21]" and \( r2 \) is encoded in "instruction[20-16]" ("instruction[0-15]" are not used). The "js" instruction is a special subroutine call instruction. It causes PC+4 to be stored in \( r1 \) and it copies \( r2 \) into the PC. The result is a jump to the memory location whose address is in \( r2 \) while preserving the return address. Add any necessary datapaths and control signals to the architecture of Figure 5.17.