Question 1 (25 Points)
Consider two machines A and B. Machine A does not have floating point hardware and implements floating point instruction in software. It takes 30 and 40 Integer instructions to implement a floating point add (FADD) instruction and a floating point Divide (FDIV) instruction, respectively, on machine A. Machine B, on the other hand, has floating point hardware to directly execute FADD and FDIV. An integer instruction executes in one clock cycle on both machines, and FADD and FDIV execute in 5 and 8 clock cycles, respectively, on machine B. Consider a program which has 200 million instructions and the following mix of instructions:

- 10% FDIV
- 20% FADD
- 70% Integer instructions

a. How many clock cycles will it take to execute the program on each of machines A and B?
b. How long will it take to execute the program on each of machines A and B, assuming 1 GHz (1000 MHz) clock rate.
c. How many native instructions will each machine execute? A native instruction is one that executes directly on the hardware. Note that machine A does not execute FDIV and FADD directly on the hardware, but rather executes 30 native instructions for each FADD and 40 native instructions for each FDIV.
d. Compute MIPS rating (the number of million native instructions executing per second) for each machine.

Question 2 (25 Points)
Consider a MIPS program with the following mix of instructions

- 40% R-type arithmetic instructions
- 25% lw instructions
- 20% sw instructions
- 10% beq and bne instructions
- 5% Jump instructions

a. What percentage of all memory accesses during the execution of this program are for data (as opposed to instructions) and what percentage of all memory accesses are reading from memory (as opposed to writing to memory)?
b. Assume that the instruction mix for this program is typical of all the programs that execute on a 1 GHz machine in which the R-type instructions execute in 6 cycles, the lw and sw instructions in 4 cycles, the beq and bne instructions in 3 cycles and the jump instructions in 2 cycles. What is the MIPS (million instructions per second) rate for that machine?
c. Assume that it is possible to change the architecture so as to save one cycles from the execution of each instruction. That is the R-type instructions execute in 5 cycles, the lw and sw instructions in 3 cycles, the beq and bne instructions in 2 cycles and the jump instructions in 1 cycle. This architecture change, however, will require that the machine operates at 800MHz rather than 1GHz. Would you recommend that change? Justify your answer.
Question 3 (25 Points)
Do problem 4.8 from text.

Question 4 (25 Points)
Do problem 4.10 from text

Due Wednesday September 27, 2006