EGE320 Electronics I (3 credits)
Fall 2011 Semester

COURSE SYLLABUS

1. GENERAL INFORMATION

Professor: Dr. Julio J. González

Office: REH 113
Voice mail: (845) 257-3724, Fax: (845) 257-3730
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Office hours: Tuesday 10:00 AM – 12:00 PM,
Wednesday 01:00 PM – 03.00 PM

Textbook: "Microelectronic Circuits" by Sedra and Smith,
6th edition, Oxford University Press, 2010.

2. DESIRED LEARNING OUTCOMES

Students will demonstrate their ability to:

I. learn the operation principle and modeling of operational amplifiers (as a "black box"), diodes, zener diodes, bipolar transistors and field effect transistors, and apply this knowledge to the analysis of circuits containing the aforementioned devices, both in the time domain and the frequency domain

II. Design electronic circuits in the time domain and the frequency domain by working in a design team, and

3. STUDENT OUTCOMES

This course contributes to the Student Outcomes specified in the following table:

Student Outcome	Course Desired Learning Outcome	Level of Contribution 3 = strong; 2 = moderate; 1 = marginal
a) An ability to apply knowledge of mathematics, science and engineering	I	3
e) An ability to identify, formulate and solve engineering problems	II	3

4. COURSE CONTENTS

The operational amplifier as a “black box”; Operational Amplifier circuits; Ideal and real diode: Physical operation, DC and AC Models, rectifier circuits. Bipolar Junction Transistor (BJT): Physical operation, DC model and biasing, AC model and amplification; Amplifier circuits, gain, input and output resistance; Field Effect Transistors (FET’s): Physical Operation; DC model and biasing; AC model and amplification; Amplifier circuits, gain, input and output resistance

5. TENTATIVE SCHEDULE FOR TOPICS

WEEK	TOPIC
1,2	The operational amplifier as a “black box”; Operational Amplifier circuits
3, 4	Ideal and real diode: Physical operation, DC and AC Models, rectifier circuits
5, 6	Bipolar Junction Transistor (BJT): Physical operation
7	BJT: DC model and biasing
8, 9	BJT: AC model and amplification; Amplifier circuits, gain, input and output resistance
10, 11	Field Effect Transistors (FET’s): Physical Operation
12	BJT: DC model and biasing
13, 14	BJT: AC model and amplification; Amplifier circuits, gain, input and output resistance

6. SCHEDULE FOR EXAMINATIONS, PROJECTS AND HOMEWORK

Event	Date Assigned	Date due
Homework 1,2	08/29	09/12
Homework 3	09/12	09/19
Homework 4	09/19	09/26
Homework 5	09/26	10/03
Homework 6	10/03	10/11
First Partial Examination	**10/13**	**10/13**
Homework 7	10/17	10/24
Homework 8	10/24	10/31
Homework 9	10/31	11/07
Homework 10	11/07	11/14
Second Partial Examination	**11/18**	**11/18**
Design Project	11/21	12/12
Homework 11	11/21	11/28
Homework 12	11/28	12/05
Final Examination	**12/15**	**12/15**

NOTES:

- The partial examinations will take place from 01:40 PM to 02:55 PM
- The final examination will take place from 12:30 PM to 02:30 PM
- The project and homework assignments will be due at 01:40 PM of the corresponding date.

5. GRADING POLICY

5.1. Grade Distribution

Homework:	15%
Project:	20%
First Midterm Exam:	20%
Second Midterm Exam:	20%
Final Exam:	25%

Total:	100%

NOTE: The course will be automatically failed if any of the following conditions apply:

- *Failing to take any of the three examinations*
- *Failing to present the project report*
- *Obtaining less than a passing grade (55%) in the project report, or in more than one examination. Obtaining less than a 55% average in the homework.*

5.2. Grading discrepancy

In case of grading discrepancy, the student should see the grader within a week from the date he/she receives the graded document. After this period of time has elapsed, grades will not be changed.

5.3. Class Attendance

Attendance to classes is strongly encouraged. The grade will be negatively affected when more than three unjustified missed classes occur.