

SUNY NEW PALTZ
Department of Electrical and Computer Engineering

EGC446 VLSI Design Laboratory (1 credit)
Spring 2017

Wednesday: 2.00 - 4.50PM, WH221

COURSE SYLLABUS

1. GENERAL INFORMATION

Instructor: Dr. Damu Radhakrishnan

Office: REH 204
Voice mail: (845) 257-3772
Fax: (845) 257-3730
E-mail: damu@enr.newpaltz.edu
Office hours: Wednesday 12:30 - 1:45PM

Textbook: John P. Uyemura, **Introduction to VLSI Circuits and Systems**, John Wiley & Sons, Inc., 2002

John P. Uyemura, Chip Design for Submicron VLSI:
CMOS Layout and Simulation, Thomson, 2006

2. COURSE DESCRIPTION (as it appears in the current catalog)

Static and dynamic characteristics of CMOS logic gates. Design of CMOS circuits using transistor schematics, and verification through simulation. Layout of CMOS circuits using state-of-the-art VLSI tools, design rule check, and verification through simulation.

3. STUDENT LEARNING OUTCOMES

- I. Students will learn the behavior of CMOS logic circuits, both combinational and sequential, through SPICE simulation and verify their static and dynamic characteristics.
- II. Students will use state-of-the-art IC design tools to design CMOS integrated circuits by creating transistor schematics and manual layout satisfying MOSIS design rules, and verify their performance by netlist extraction and simulation.

III. Students will enhance their professional writing skills by creating clear and concise laboratory reports.

4. ABET PROGRAM OUTCOMES

- (a) an ability to apply knowledge of mathematics, science, and engineering
- (b) an ability to design and conduct experiments, as well as to analyze and interpret data
- (c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability
- (d) an ability to function on multidisciplinary teams
- (e) an ability to identify, formulate, and solve engineering problems
- (f) an understanding of professional and ethical responsibility
- (g) an ability to communicate effectively
- (h) the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context
- (i) a recognition of the need for, and an ability to engage in life-long learning
- (j) a knowledge of contemporary issues
- (k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

5. COURSE CONTRIBUTION TO STUDENT LEARNING OUTCOMES

This lab contributes to ABET program outcomes as specified in the following table:

Student outcome	Course learning outcome	Level of contribution 3/3 = strong; 2/3 = moderate; 1/3 = marginal
b) An ability to design and conduct experiments, as well as to analyze and interpret data	II	3/3
g) An ability to communicate effectively	III	2/3
k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	I, II	3/3

6. COURSE CONTENTS

SPICE simulation of inverter, NAND and NOR gate.
Transistor schematics of logic gates and their netlist extraction.
Layout of CMOS gates, design rule checking, layout vs schematics, extraction, and Spice simulation. Standard cell layouts.

Layout design and performance verification of XOR/XNOR gates and full adder cells. Quasi-static latch and binary counter in CMOS technology.

Tools used: SPICE, Electric VLSI Design software

7. GRADING POLICY

7.1. Grade Distribution

Final Lab reports:	60%
Work Book:	30%
Attendance:	10%

Total:	100%

7.2. Grade Discrepancy

Any disputed grade must be resolved within 7 days of the return of the graded item.

7.3. Class Performance

Regular laboratory attendance is very important for the successful completion of the course. **10% of the final grade is assigned to lab attendance.**

You should use a **lab notebook** for this course. You should come prepared for the lab by doing all preliminary work at home. Draw all circuit diagrams, stick diagrams and rough layout in you notebook. Take notes in your lab notebook as you do things so that you can easily refer to them later without wading through the long lab handouts. **30% of your final grade is assigned to lab notebook. Instructor will grade your lab notebook regularly during the course of the semester.**

You will write final lab reports for most laboratories.

Academic Integrity Statement (From Student Catalog)

Students are expected to maintain the highest standards of honesty in their college work. Cheating, forgery, and plagiarism are serious offenses, and students found guilty of any form of academic dishonesty are subject to disciplinary action.

Cheating is defined as giving or obtaining information by improper means in meeting any academic requirements. The use for academic credit of the same work in more than one course without knowledge or consent of the instructor(s) is a form of cheating and is a serious violation of academic integrity.

Forgery is defined as the alteration of college forms, documents, or records, or the signing of such forms or documents by someone other than the proper designee.

Plagiarism is the representation, intentional or unintentional, of someone else's words or ideas as one's own. Since words in print are the property of an author or publisher, plagiarizing is a form of larceny punishable by fine. When using another person's words in a paper, students must place them within quotation marks or clearly set them off in the text and give them appropriate footnoting. When students use only the ideas and change the words, they must clearly identify the source of the ideas. Plagiarism, whether intentional or unintentional, is a violation of the property rights of the author plagiarized and of the implied assurance by the students when they hand in work that the work is their own.

Faculty members are responsible for making the initial determination of the academic penalty to be imposed in cases of cheating, plagiarism, or forgery and for informing the department chair, the dean and the student in writing of the alleged violation and proposed penalty. The academic penalty may range, for instance, from a reprimand accompanied by guidance about how to avoid plagiarism in the future to failure for the course. The academic dean may request that the Dean of Students send a follow-up letter to the student indicating that they have also been notified of the academic integrity violation and that subsequent violations will lead to judicial action.

If a student has any question about what constitutes a violation of academic integrity, it is that student's responsibility to clarify the matter by conferring with the instructor and to seek out other resources available on the campus. The link regarding plagiarism on the Sojourner Truth Library's website is an excellent beginning, <http://lib.newpaltz.edu/assistance/plag.html>.

Reasonable accommodation of individuals with disabilities statement

Any student who will need classroom and/or testing accommodations based on the impact of a disability should contact the Disability Resource Center, Student Union, Room 210, 845-257-3020. The DRC will provide an Accommodation Memo for your instructors verifying the need for accommodations. Students are encouraged to request accommodations as close to the beginning of the semester as possible.

Information on electronic SEIs

You are responsible for completing the Student Evaluation of Instruction (SEI) for this course. I value your feedback and use it to improve my teaching and planning. Please complete the form during the open period on-line [**April 26 – May 10, 2017**].

Important dates

Last day to withdraw from a course without receiving a penalty grade: March 31, 2017.