

# Conference papers

- B. Jose and **D. Radhakrishnan**, [Fast Redundant Binary Partial Product Generators for Booth Multiplication](#), Proc. 50<sup>th</sup> IEEE International Midwest Symp. on Circuits and Systems, Montreal, Canada, pp. 297-300, Aug. 2007.
- Yu Shen Lin and **D. Radhakrishnan**, [Delay Efficient 32-bit Carry-skip Adder](#), Proc. 13<sup>th</sup> IEEE International Conference on Electronics, Circuits and Systems, Nice, France, pp. 506-507, Dec. 2006.
- B. Jose and **D. Radhakrishnan**, [Delay Optimized Redundant Binary Adders](#), Proc. 13<sup>th</sup> IEEE International Conference on Electronics, Circuits and Systems, Nice, France, pp. 514-517, Dec. 2006.
- Y. Liu, E.M-K. Lai, A.B. Premkumar and **D. Radhakrishnan**, [A Low-Power Pipelined Implementation of 2D Discrete Wavelet Transform](#), Proc. International Conference on Embedded Systems and Applications, pp. 40-46, Las Vegas, Nevada, June 2004.
- Jayapreetha Natesan and **D. Radhakrishnan**, [Shift Invert Coding \(SINV\) for Low Power VLSI](#), Proc. Euromicro Symposium on Digital System Design (DSD04), pp. 190-194, Rennes, France, Aug-Sept. 2004.
- R.V. Menon, S. Chennupati, N.K. Samala, **D. Radhakrishnan** and B. Izadi, [Switching Activity Minimization in Combinational Logic Design](#), Proc. International Conference on Embedded Systems and Applications, pp. 47-53, Las Vegas, Nevada, June 2004.
- Naveen K. Samala, **D. Radhakrishnan**, and Baback Izadi, [A Novel Deep Sub-micron Bus Coding for Low Energy](#), Proc. International Conference on Embedded Systems and Applications, pp. 25-30, Las Vegas, Nevada, June 2004.
- Smith Castillo, Naveen K. Samala, Kerron Manwaring, Baback Izadi and **D. Radhakrishnan**, [Experimental Analysis of Batteries Under Continuous and Intermittent Operations](#), Proc. International Conference on Embedded Systems and Applications, pp. 18-24, Las Vegas, Nevada, June 2004.
- Jayapreetha Natesan and **D. Radhakrishnan**, [A Novel Bus Encoding Technique for Low Power VLSI](#), Proc. International Conference on Embedded Systems and Applications, pp. 54-62, Las Vegas, Nevada, June 2004.
- S.K. Bhaskaran, R.W. Sobhitha and **D. Radhakrishnan**, [A Simple and Efficient State Code Assignment Algorithm](#), Proc. 7<sup>th</sup> IEEE International Symp. on Consumer Electronics (ISCE-2003), Sidney, Australia, Dec. 2003.
- M.L. Gardner, L. Yu, J.W. Muthumbi, O.B. Mbowe, **D. Radhakrishnan** and A.P. Preethy, [ROM Efficient Logarithmic Addition in RNS](#), Proc. 7<sup>th</sup> IEEE International Symp. on Consumer Electronics (ISCE-2003), Sidney, Australia, Dec. 2003.
- H. Yang, Y. Sun, **D. Radhakrishnan** and A.P. Preethy, [A Novel Technique for Low Energy Adaptive Bus Coding](#), Proc. 7<sup>th</sup> IEEE International Symp. on Consumer Electronics (ISCE-2003), Sidney, Australia, Dec. 2003.
- S. Uppaluri, B. Izadi and **D. Radhakrishnan**, [Low Power Dynamic Scheduling in](#)

[Heterogeneous Systems](#), Proc. International Conference on Embedded Systems and Applications, Las Vegas, Nevada, pp. 261-267, June 2003.

- R.V. Menon, S. Chennupati, N.K. Samala, **D. Radhakrishnan** and B. Izadi, [Power Optimized Combinational Logic Design](#), Proc. International Conference on Embedded Systems and Applications, Las Vegas, Nevada, pp. 223-227, June 2003.
- **D. Radhakrishnan**, [Low Power 4-2 Compressor with Fully Restored Node Voltages](#), 5<sup>th</sup> WSES Intl. Conf. on Circuits, Systems, Communications and Computers (CSCC 2001), Rethymno, Greece, pp. 5811-5816, July 2001.
- A.P. Preethy, **D. Radhakrishnan** and A. Omondi, [Fault-Tolerance Scheme for an RNS MAC: Performance and Cost Analysis](#), IEEE Intl. Symp. on Circuits and Systems (ISCAS 2001), Sydney, Australia, vol. 2, pp. 717-720, May 2001.
- A.P. Preethy, **D. Radhakrishnan** and A. Omondi, [A High Performance RNS Multiply-Accumulate Unit](#), Proc. 11<sup>th</sup> Great Lakes Symp. on VLSI (GLSVLSI 2001), West Lafayette, Indiana, pp. 145-148, March 2001.
- A.P. Preethy and **D. Radhakrishnan**, Architectures for Logarithmic Addition in Integer Rings and Galois Fields, WSES 2000 Conf. on Algorithms Theory, Discrete Mathematics, Systems and Control, Athens, Greece, Dec. 2000.
- J. Mathew and **D. Radhakrishnan**, [An FIR Digital Filter Using One-Hot Coded Residue Representation](#), European Signal Processing Conf. (EUSIPCO-2000), Tampere, Finland, vol. iv, pp. 1885-1888, Sept. 2000.
- **D. Radhakrishnan** and A.P. Preethy, [Low Power CMOS Pass Logic 4-2 Compressor for High Speed Multiplication](#), The 43<sup>rd</sup> Midwest Symp. on Circuits and Systems (MWSCAS2000), Michigan, USA, Aug. 2000.
- F.P. Ling, F.K. Khuen and **D. Radhakrishnan**, [An Audio Processor Card for Special Sound Effects](#), The 43<sup>rd</sup> Midwest Symp. on Circuits and Systems (MWSCAS2000), Michigan, USA, Aug. 2000.
- **D. Radhakrishnan**, [Pass Logic Circuits with Reduced Switching Activity for Low Power DSP Processors](#), Intl. Conf. on Acoustics, Speech, and Signal Processing (ICASSP2000), Istanbul, Turkey, vol. 6, pp. 3327-3330, June 2000.
- **D. Radhakrishnan**, [Low Power Arithmetic Units Using Pass Logic](#), Fourth Intl. Conf. on High Performance Computing (HPC-Asia 2000), Beijing, China, vol. 1, pp. 332-336, May 2000.
- J. Mathew and **D. Radhakrishnan**, [A High Speed RNS FIR Digital Filter Architecture with Totally Self Checking Code Error Detection](#), Second Intl. Conf. Information, Communications & Signal Processing, Singapore, 2B3, no. 5, Dec. 1999.
- **D. Radhakrishnan**, [A New Low Power CMOS Full Adder](#), IEEE Malaysia International Conf. on Communications and IEEE Asia Pacific International Symp. on Consumer Electronics, Malaysia, vol. 2, pp. 154-157, Nov. 1999.
- **D. Radhakrishnan**, [Formal Design Procedures for Differential Cascode Voltage Switch with Pass Gate \(DCVSPG\) Logic](#), IEEE Malaysia International Conf. on Communications and IEEE Asia Pacific International Symp. on Consumer Electronics, Malaysia, vol. 2, pp. 238-241, Nov. 1999.
- J. Mathew, **D. Radhakrishnan** and T. Srikanthan, [Residue-to-Binary Arithmetic Converter for the Moduli Set  \$\{2^{n+1}, 2^n, 2^n-1, 2^{n+1}+1, 2^{n+2}-1\}\$](#) , Proc. Tenth Annual Intl. Conf. Signal

Processing Applications and Technology (ICSPAT99), Orlando, Florida, pp. 1076-1080, Nov. 1999.

- K.V. Asari, **D. Radhakrishnan** and S. Kumar, Correction of Barrel Distortion in Endoscopic Images using  $L_2$ -Norm Approximation, Proc. IASTED Intl. Conf. Intelligent Systems and Control - ISC'99, Santa Barbara, California, pp. 339-340, Oct. 1999.
- C.K. Yew, C. T. Boon, F.P. Ling, T.Y. Sai, K.V. Asari and **D. Radhakrishnan**, [A Digital Neuro-chip Design for an ART Based Self-organizing Neural Network](#), 5<sup>th</sup> NUROP Congress, NTU, Singapore, Sept. 1999.
- J. Mathew, **D. Radhakrishnan**, and T. Srikanthan, [New Area Efficient Residue-to-Weighted Number System Converters](#), IEEE Intl. Conf. Electronics, Circuits and Systems (ICECS '99), Pafos, Cyprus, vol. II, pp. 945-948, Sept. 1999.
- J. Mathew and **D. Radhakrishnan**, Residue-to-Mixed Radix Converter with Totally Self-Checking Code Error Detection, Eighth Intl. Symp. Integrated Circuits, Devices & Systems (ISIC-99), Singapore, pp. 483-485, Sept. 1999.
- A.P. Preethy and **D. Radhakrishnan**, [A Single Fault Tolerant Multiplier for RNS Applications](#), Eighth Intl. Symp. Integrated Circuits, Devices & Systems (ISIC-99), Singapore, pp. 486-489, Sept. 1999.
- J. Mathew, **D. Radhakrishnan**, and T. Srikanthan, Memoryless Fully Parallel Residue-to-Mixed Radix Converter, European Conf. Circuit Theory and Design (ECCTD '99), Torino, Italy, pp. 707-710, Aug.-Sept. 1999.
- A.P. Preethy and **D. Radhakrishnan**, [A 36-bit Balanced Moduli MAC Architecture](#), 42<sup>nd</sup> Midwest Symp. on Circuits and Systems (MWSCAS99), Las Cruces, NM, vol. 1, pp. 380-383, Aug. 1999.
- J. Mathew, **D. Radhakrishnan** and T. Srikanthan, Fast Residue-to-Binary Converter Architectures, 42<sup>nd</sup> Midwest Symp. on Circuits and Systems (MWSCAS99), Las Cruces, NM, vol. 2, pp. 1090-1093, Aug. 1999.
- S. Kumar, K.V. Asari, and **D. Radhakrishnan**, A New Technique for the Segmentation of Lumen from Endoscopic Images by Differential Region Growing, 42<sup>nd</sup> Midwest Symp. on Circuits and Systems (MWSCAS99), Las Cruces, NM, vol. 1, pp. 414-417, Aug. 1999.
- A.P. Preethy and **D. Radhakrishnan**, [A VLSI Architecture for Analog-to-Residue Conversion](#), 3rd Intl. Conf. on Advanced A/D and D/A Conversion Techniques and Their Applications, Glasgow, UK, pp. 83-85, July 1999.
- **D. Radhakrishnan**, T. Srikanthan and J. Mathew, [Using the  \$2^n\$  Property to Implement an Efficient General Purpose Residue-to-Binary Converter](#), Proc. Intl. Symp. Signals, Circuits and Systems (SCS '99), Iasi, Romania, pp. 183-186, July 1999.
- J. Mathew, **D. Radhakrishnan**, T. Srikanthan and A.P. Preethy, [A Low Overhead Reverse Converter for Fault Tolerant RNS](#), 1999 Intl. Tech. Conf. Circuits/Systems, Computers and Communications, Niigata, Japan, vol. II, pp. 767-770, July 1999.
- S. Kumar, K.V. Asari, and **D. Radhakrishnan**, [Online Extraction of Lumen Region and Boundary from Endoscopic Images using a Quad Structure](#), 7<sup>th</sup> Intl. Conf. Image Processing and its Applications, vol. 2, pp. 818-822, Manchester, UK, July 1999.
- K.V. Asari, T. Srikanthan, S. Kumar, and **D. Radhakrishnan**, [A Systolic Architecture for Image Segmentation by Adaptive Progressive Thresholding](#), 7<sup>th</sup> Intl. Conf. Image Processing and its

Applications, vol. 1, pp. 107-111, Manchester, UK, July 1999.

- J. Mathew, **D. Radhakrishnan** and T. Srikanthan, [Residue-to-Binary Arithmetic Converter for the Moduli Set  \$\{2^n-1, 2^n, 2^n+1, 2^{n+1}-1\}\$](#) , 1999 IEEE-EURASIP Workshop on Nonlinear Signal and Image processing (NSIP'99), pp. 190-193, Antalya, Turkey, June 1999.
- J. Mathew and **D. Radhakrishnan**, A High Speed RNS Processor with TSC Code Error Detection, Proc. Int. Symp. Fault Tolerant Computing - FTCS29 Fast Abstracts, pp. 55-56, Madison, Wisconsin, June 1999.
- **D. Radhakrishnan** and A.P. Preethy, [A Novel 36-bit Single Fault Tolerant Multiplier using 5-bit Moduli](#), IEEE Intl. Conf. Global Connectivity in Energy, Computer, Communication and Control (TENCON 98), pp. 128-130, vol. I, New Delhi, India, Dec. 1998.
- **D. Radhakrishnan** and A.P. Preethy, [A Direct Analog-to-Residue Converter](#), IEEE Intl. Conf. Global Connectivity in Energy, Computer, Communication and Control (TENCON 98), pp. 336-339, vol. II, New Delhi, India, Dec. 1998.
- **D. Radhakrishnan** and A.P. Preethy, A 20-bit Subranging Analog-to-Residue Converter, 3<sup>rd</sup> High Performance Computing ASIA Conf., pp. 287-290, Singapore, Sept. 1998.
- **D. Radhakrishnan** and A.P. Preethy, [A 32-bit Multiplier Architecture Using Galois Fields](#), The 2<sup>nd</sup> IASTED European Conf. Parallel and Distributed Systems, pp. 94-99, Vienna, Austria, July 1998.
- **D. Radhakrishnan** and A.P. Preethy, [A New Approach to Data Conversion: Direct Analog-to-Residue Converter](#), Intl. Conf. on Acoustics, Speech and Signal Processing, vol. 5, pp. 3013-3016, Seattle, USA, May 1998.
- **D. Radhakrishnan** and A.P. Preethy, [Novel Galois Field Techniques for a 32-bit Superset Modulo Multiplier](#), The 3<sup>rd</sup> Intl. Conf. On Massively Parallel Computing Systems, Colorado Springs, USA, April 1998.
- T. Srikanthan and **D. Radhakrishnan**, [VLSI Efficient Binary-to-Residue Converter for DSP Applications](#), Proc. Intl. Symp. On Communication Systems and Digital Signal Processing, pp. 151-153, Sheffield, UK, April 1998.
- K.S. Manjunath and **D. Radhakrishnan**, [Transition Count Testing of CMOS Combinational Circuits](#), First Great Lakes Symp. VLSI, pp. 110-114, 1991.
- **D. Radhakrishnan** and T. Pyon, [Fault Tolerance in RNS: An Efficient Approach](#), Proc. IEEE Intl. Conf. on Computer Design: VLSI in Computers & Processors, pp. 41-44, Sept. 1990.
- **D. Radhakrishnan** and C. Lai, [Efficient Test Generation for CMOS Circuits](#), Proc. 33rd Midwest Symp. on Circuits and Systems (MWSCAS90), vol. 1, pp. 588-591, Aug. 1990.
- **D. Radhakrishnan** and Y. Yuan, [A Fast RNS Galois Field Multiplier](#), Proc. IEEE Intl. Symp. on Circuits and Systems, vol. 4, pp. 2909-2912, May 1990.
- V. Bobin and **D. Radhakrishnan**, [A VLSI Residue Arithmetic Multiplier with Fault Detection Capability](#), Proc. IEEE Intl. Conf. on Computer Design: VLSI In Computers & Processors, pp. 348-351, Oct. 1989.
- J.A. Jacksha, **D. Radhakrishnan** and G.K. Maki, Reverse Testing of NMOS Binary Tree Structured Networks, Proc. 21st Annual Asilomar Conf. on Signals, Systems and Computers, pp. 525-530, Nov. 1987.

- A. Feizi and **D. Radhakrishnan**, Multiple Output Pass Networks: Design and Testing, Proc. IEEE Intl. Test Conf., pp. 907-911, Nov. 1985.
- **D. Radhakrishnan** and R. Sharma, Easily Testable CMOS Cellular Arrays for VLSI, Proc. IEEE Intl. Conf. on Computer Design: VLSI in Computers, pp. 426-429, Oct. 1985.
- A. Feizi and **D. Radhakrishnan**, High Performance Switching Circuits for VLSI, Proc. IEEE Intl. Conf. on Computer Design: VLSI in Computers, pp. 53-56, Oct. 1985.
- **D. Radhakrishnan** and R. Sharma, Test Derivation for CMOS Iterative Logic Arrays, Proc. Custom Integrated Circuits Conf., pp. 315-318, May 1985.
- R. Sharma and **D. Radhakrishnan**, Test Derivation for Stuck-open Faults in Iterative Logic Arrays, Proc. 22nd Annual Allerton Conf. on Communication, Control and Computing, pp. 844-853, Oct. 1984.
- **D. Radhakrishnan**, S.R. Whitaker and G.K. Maki, Formal Design Procedures for Pass Transistor Switching Circuits, Proc. Custom Integrated Circuits Conf., pp. 139-144, May 1984.
- **D. Radhakrishnan** and G. Maki, Test Derivation for MOS Switch Logic Networks, Proc. 21st Annual Allerton Conf. on Communication, Control and Computing, pp. 786-795, Oct. 1983.