SUNY NEW PALTZ
Department of Electrical and Computer Engineering

EGC445/EGE537 VLSI Design (3 credits)
Spring 2017 Semester

1. GENERAL INFORMATION

Instructor: **Damu Radhakrishnan**, 204 Resnick Engineering Hall
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Lecture:	Tuesday/Friday	9.30 – 10.45PM, REH111
Lab:	Wednesday	2.00 – 4.50PM, WH221
Office Hours:	Tuesday	11.00 – 12.15PM

Textbook: John P. Uyemura, **Introduction to VLSI Circuits and Systems**, John Wiley & Sons, Inc., 2002

Reference Texts: John P. Uyemura, **Chip Design for Submicron VLSI: CMOS Layout and Simulation**, Thomson, 2006
Etienne Sicard and Sonia Delmas Bendhia, **Basics of CMOS Cell Design**, McGraw-Hill, 2007
Jan M. Rabaey, A. Chandrakasan, and B. Nikolic, **Digital Integrated Circuits - A Design Perspective**, Prentice-Hall, 2003
Neil H.E. Weste and David Harris, **CMOS VLSI Design – A Circuits and Systems Perspective**, 4nd Edition, Pearson, 2010
Ken Martin, **Digital Integrated Circuit Design**, Oxford University Press, 2000
Dan Clein, **CMOS IC Layout**, Concepts, Methodologies, and Tools, Newnes, 2000
Jacob Baker, **CMOS Circuit Design, Layout, and Simulation**, Wiley 2010

Prerequisites: Digital Logic Fundamentals (EGC220), Electronics 1 (EGE320). Students are expected to know logic design, elementary circuits and device physics from sophomore and junior-level courses. Some background in computer organization is helpful, but not required. Electric VLSI design tools and Spice simulation are heavily used in the lab.

2. COURSE DESCRIPTION (as it appears in the current catalog)

Introduction to CMOS, MOS transistor theory. IC technology and layout design rules. Design of CMOS circuits. Circuit characterization and performance estimation. Memory, clocking and input/output circuits. Microarchitecture of VLSI systems. Chip design projects. Testability.

3. STUDENT LEARNING OUTCOMES

I. Learn and understand MOS transistor and CMOS circuit operation and analyze CMOS logic circuits by verifying their logical, static and dynamic behavior.

II. Design CMOS logic circuits, both simple and complex ones, using complementary CMOS, pass logic, transmission gates and dynamic logic styles. Do the layout of CMOS circuits satisfying design rules, perform DRC, extract parasitics and measure the performance using CAD tools. These design activities culminate in a course design project and the corresponding project report.

Mapping between the ABET Program Outcomes and this Course

Student outcome	**Course learning outcome**	**Level of contribution** **3/3 = strong;** **2/3 = moderate;** **1/3 = marginal**
a) An ability to apply knowledge of mathematics, science and engineering	I	3/3
e) An ability to identify, formulate and solve engineering problems	II	3/3

4. COURSE CONTENTS`

Introduction - MOSFET operation.
Fabrication process – nmos, pmos and cmos transistors.
Design rules – MOSIS design rules, Layout design and software tools.
CMOS Inverter - Definitions and properties, Static behavior, Delay characteristics, Power consumption.
CMOS Logic Gates - Static CMOS Design, Dynamic CMOS Design, Domino logic, CVSL.
Interconnects - capacitive and resistive parasitics calculations.
Sequential Circuits – Analysis and design of Static and Dynamic sequential circuits.
Timing Issues - Clocking strategies in VLSI circuits, Clock generation and distribution.
Testing VLSI Circuits – Fault models, test generation. Review.
Software used: SPICE, Electric VLSI software
Materials required: graph paper, **red/green/blue/yellow/tan/grey/ black colored pencils**

5. COURSE RULES AND GENERAL COMMENTS

- **Regular class attendance is very important and attendance will be taken at the beginning of each lecture. A 5% bonus will be credited for those who attend classes regularly, and do not miss more than 2 lecture sessions during the whole semester. No bonus credit will be given otherwise. Those who come to the lecture more than 5 minutes late will be marked as absent. If you come late within the permitted 5 minute time period, it is your responsibility to make sure that your attendance is recorded properly.**
- You are responsible for all the course materials and all lecture contents unless specified otherwise by the instructor. **If you miss a class, it is your responsibility to obtain assignments and other information given on that day.**
- If you have questions on course materials, the instructor will be available for consultation. Please try to get answers before serious difficulties in your understanding of course material arise. In particular, it is much better to get your questions answered before an exam than after!
- Save your graded homework and tests. You may need to bring them in case of any grade discrepancy.
- **There is a design project for the course** (details to be discussed later). Upon completion of the project, each student is required to submit a formal report.

Please pay attention to the following requirements regarding your homework assignment:

- Always use standard size (8½ × 11) paper. Please do not use torn-off paper from spiral bound notebooks.
- Write the course #, homework #, and your name on top of the first page, as shown below

  Course # Homework # Your Name
  - Write clearly, neatly and in an orderly fashion
  - Draw block schematics, circuit diagrams, layout etc. when applicable Show all steps. No credit may be given for the work not shown.
  - **No late homework solutions will be accepted**.
  - **Please staple all homework pages together before you turn them in**.

6. GRADING

Homework	15%
Project	25%
2 Midterm Exams	30%
Quiz	10%
Final Exam	20%
Total	100%

Total (%)	**Final Grade**
90-100	A
85-89	A-
80-84	B+
75-79	B
70-74	B-
65-69	C+
60-64	C
55-59	C-
Below 55	F

Design Project Due: Tuesday May 9, 2017
Final Examination: 10.15-12.15PM, Friday May 19, 2017

Academic Integrity Statement (From Student Catalog)
Students are expected to maintain the highest standards of honesty in their college work. Cheating, forgery, and plagiarism are serious offenses, and students found guilty of any form of academic dishonesty are subject to disciplinary action.

Cheating is defined as giving or obtaining information by improper means in meeting any academic requirements. The use for academic credit of the same work in more than one course without knowledge or consent of the instructor(s) is a form of cheating and is a serious violation of academic integrity.

Forgery is defined as the alteration of college forms, documents, or records, or the signing of such forms or documents by someone other than the proper designee.

Plagiarism is the representation, intentional or unintentional, of someone else's words or ideas as one's own. Since words in print are the property of an author or publisher, plagiarizing is a form of larceny punishable by fine. When using another person's words in a paper, students must place them within quotation marks or clearly set them off in the text and give them appropriate footnoting. When students use only the ideas and change the words, they must clearly identify the source of the ideas. Plagiarism, whether intentional or unintentional, is a violation of the property rights of the author plagiarized and of the implied assurance by the students when they hand in work that the work is their own.

Faculty members are responsible for making the initial determination of the academic penalty to be imposed in cases of cheating, plagiarism, or forgery and for informing the department chair, the dean and the student in writing of the alleged violation and proposed penalty. The academic penalty may range, for instance, from a reprimand accompanied by guidance about how to avoid plagiarism in the future to failure for the course. The academic dean may request that the Dean of Students send a follow-up letter

to the student indicating that they have also been notified of the academic integrity violation and that subsequent violations will lead to judicial action.

If a student has any question about what constitutes a violation of academic integrity, it is that student's responsibility to clarify the matter by conferring with the instructor and to seek out other resources available on the campus. The link regarding plagiarism on the Sojourner Truth Library's website is an excellent beginning, http://lib.newpaltz.edu/assistance/plag.html.

Reasonable accommodation of individuals with disabilities statement

Any student who will need classroom and/or testing accommodations based on the impact of a disability should contact the Disability Resource Center, Student Union, Room 210, 845-257-3020. The DRC will provide an Accommodation Memo for your instructors verifying the need for accommodations. Students are encouraged to request accommodations as close to the beginning of the semester as possible.

Information on electronic SEIs

You are responsible for completing the Student Evaluation of Instruction (SEI) for this course. I value your feedback and use it to improve my teaching and planning. Please complete the form during the open period on-line [**April 26 – May 10, 2017**].

Important dates

Last day to withdraw from a course without receiving a penalty grade: March 31, 2017.