

# A Novel Deep Sub-micron Bus Coding for Low Energy

Naveen K. Samala, Damu Radhakrishnan and Baback Izadi  
Department of Electrical and Computer Engineering  
State University of New York  
New Paltz, New York 12561  
samala49@newpaltz.edu, {damu, bai}@enr.newpaltz.edu

## Abstract

*In modern digital circuits the total power attributed to wires is increasing. Reducing the power consumption in wires play a major role in low power design. Coupling transitions contribute to significant energy loss in deep sub-micron buses. Earlier schemes using the switching activity minimization based upon the substrate capacitances are not valid in these buses. Hence, a new low energy bus-encoding scheme is proposed which showed 10 % reduction in coupling transitions for 8 and 16 bit data.*

Keywords: Bus, Coupling Transition, Self-Transition, Coding, Decoding.

## 1. Introduction

In many digital processors the power dissipation in the bus is a major part of the total chip power dissipation. For CMOS circuits most power is dissipated as dynamic power for charging and discharging node capacitances. These capacitances are mainly the substrate capacitances of the bus wires. In these buses the power dissipation due to a transition on a bus wire is equal to  $P = T_a C_s V_{DD}^2 f / 2$ , where  $C_s$  is the substrate capacitance,  $T_a$  is the transition activity of the bus wire,  $f$  is the data transmission rate and  $V_{DD}$  is the supply voltage. Several power reduction methods for bus data transfer have been proposed [1,2,3,4,5,6]. All these methods focus on reducing the number of bus transitions. Stan and Burleson employed bus invert coding for a bus whose wires are far apart [1]. In his method, the total number of transitions occurring between the newly arrived data and the present data on the bus is first calculated. If this number is more than half the number of bus wires, then the data is inverted and sent on the bus. Otherwise, the data

is sent as is.

As the spacing between wires is getting closer and closer (deep sub-micron technology), the effect of the inter-wire (coupling) capacitances becomes more dominant that it even surpasses the substrate (base) capacitance of a wire. Therefore, in the presence of these coupling effects, earlier methods of power reduction by minimizing the switching activities based only upon substrate capacitance of a bus may not achieve their intended goal. Hence, encoding mechanisms for bus energy reduction that only rely on minimizing the number of transitions are not efficient any more.

The coupling capacitance depends on the switching behavior of a wire by taking into account its neighbors. Consider three wires as shown in Figure 1 with minimum spacing between adjacent wires. The case shown illustrates simultaneous switching on all three wires. The middle wire is shown in bold to indicate that it is switching in one direction (low to high), while the outer two wires are shown in non-bold to indicate their switching in the opposite direction (high to low). In such a case, the effective coupling capacitance gets doubled compared to the case when the neighbors are quiet. On the other hand, if all three wires are switching in the same direction (low to high) as shown in Figure 2, then the coupling capacitance becomes effectively zero.

One of the obvious ways to reduce the coupling capacitance is to increase the distance between adjacent wires, which is in contradiction to deep sub-micron technology. Another way to reduce the coupling effects is to carefully encode the data before being sent on the bus. Sotiriadis et

al have extended the work on encoding bus traffic to account for inter-wire capacitances in deep sub-micron buses by following the latter approach [7,8]. They proposed an encoding technique that attempts to

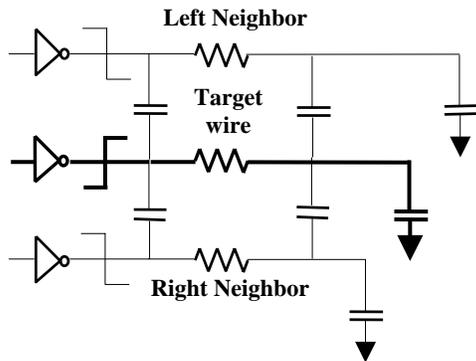


Figure 1. Cross coupling effect on the target wire from adjacent wires: Bad case

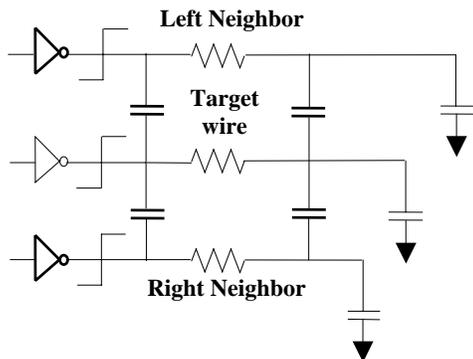


Figure 2. Cross coupling effect on the target wire from adjacent wires: Good case

minimize coupling transitions between bus wires and claimed 40% in energy savings on buses, but ignored the power consumed by the massive and complex encoding and decoding circuitry that would surpass the energy savings by a huge amount. Here, in this paper we propose a bus encoding technique for reduction of energy consumption on on-chip deep sub-micron buses while overcoming the above limitation by reducing the complex encoding and decoding circuitry with a small and simple circuitry with minimum extra power consumption.

## 2. Coding Scheme

Our coding scheme is based on the number of coupling transitions occurring on the bus when a new data is to be transmitted. The transitions occurring on a bus are generally classified into two types: self-transitions and coupling transitions. A self-transition is said to occur whenever a bus wire makes a transition from 0 to 1 or from 1 to 0. When this happens the substrate capacitance either charges from 0 to 1 or discharges from 1 to 0.

A coupling transition occurs between two adjacent bus wires, when the charge stored in the parasitic inter-wire (coupling) capacitance gets modified. For a signal transmission through a two-wire bus, all transitions between possible bit patterns and the normalized energy dissipation due to coupling capacitance are shown in Table 1. The value  $\lambda$  is defined as the ratio of coupling capacitance over substrate capacitance. The energy loss caused by the interaction of the lines through coupling capacitance is captured by  $\lambda$ . The energy consumed during a coupling transition is given by:

$$E_C = T \cdot C_s \cdot V_{DD}^2$$

where T represents  $0\lambda$ ,  $1\lambda$  and  $2\lambda$  as given in Table 1.

Table 1. Normalized energy dissipation due to coupling capacitance

Bit Pattern	00	01	10	11
00	0	$\lambda$	$\lambda$	0
01	0	0	$2\lambda$	0
10	0	$2\lambda$	0	0
11	0	$\lambda$	$\lambda$	0

In the following analysis we assume m-bit data words. The data word at time instant 'i' is denoted by  $D(i)$ . The sequence of data words  $D(0), D(1), \dots, D(k)$  are assumed to be independent and uniformly distributed. Let the input data arriving at time instant 'k' is given by:  $L(k) = \{l_1(k), l_2(k), \dots, l_m(k)\}$ . The probability of the occurrence of the data D(k) is given by:

$$P(D(k)) = \frac{1}{2^m} \forall k, m$$

When a new data vector  $D(k)$  arrives, the occurrence of  $\lambda$  and  $2\lambda$  transitions between a pair of adjacent bus wires ( $\{l_i(k-1), l_{i+1}(k-1)\}$ ) and the data ( $\{d_i(k-1), d_{i+1}(k-1)\}$ ) are given by the k-maps in Figures 3(a) and 3(b) respectively. The Boolean expression for  $\lambda$  transitions simplifies as:

$$s_i(k) = \overline{l_i(k-1)} \overline{l_{i+1}(k-1)} \overline{d_i(k)} d_{i+1}(k) + \overline{l_i(k-1)} \overline{l_{i+1}(k-1)} d_i(k) \overline{d_{i+1}(k)} + l_i(k-1) l_{i+1}(k-1) \overline{d_i(k)} d_{i+1}(k) + l_i(k-1) l_{i+1}(k-1) d_i(k) \overline{d_{i+1}(k)}$$

The total number of  $\lambda$  transitions for the complete bus is:

$$S(k) = \sum_{i=1}^{m-1} s_i(k)$$

Similarly, the Boolean expression for  $2\lambda$  transitions simplifies as:

$$r_i(k) = l_i(k-1) \overline{l_{i+1}(k-1)} \overline{d_i(k)} d_{i+1}(k) + \overline{l_i(k-1)} l_{i+1}(k-1) d_i(k) \overline{d_{i+1}(k)}$$

Hence, the total number of  $2\lambda$  transitions for the complete bus is given by:

$$R(k) = 2 \cdot \sum_{i=1}^{m-1} r_i(k)$$

The total number of coupling transitions occurring on the bus is therefore given by:

$$Q(k) = S(k) + R(k)$$

Since  $\lambda \gg 1$  in deep sub-micron busses the self-transitions on the bus are neglected.

The following procedure (Procedure 1) is now used to encode the data and send over the bus:

**Procedure 1**

1. If the calculated number of transitions  $Q(k)$  is more than half the word length, then move to the next step. Else, simply pass the data as is.
2. Calculate the Hamming Distance (HD) between the newly arrived data  $D(k)$  and the present data on the bus  $L(k-1)$  for the even lines and odd lines separately.
3. If the HD for the even lines is greater than that for the odd lines, then invert the even lines of the newly arrived data while

keeping the odd lines unchanged and pass it onto the bus.

If the HD for the odd lines is greater than that for the even lines, then invert the odd lines of the newly arrived data while keeping the even lines unchanged and pass it onto the bus.

If the HD's are equal, then invert both the even and odd lines of the newly arrived data and pass it onto the bus.

		$d_i(k) \ d_{i+1}(k)$			
		00	01	11	10
$l_i(k-1) \ l_{i+1}(k-1)$	00	0	1	0	1
	01	0	0	0	0
	11	0	1	0	1
	10	0	0	0	0

(a)  $\lambda$  Transitions

		$d_i(k) \ d_{i+1}(k)$			
		00	01	11	10
$l_i(k-1) \ l_{i+1}(k-1)$	00	0	0	0	0
	01	0	0	0	1
	11	0	0	0	0
	10	0	1	0	0

(b)  $2\lambda$  Transitions

Figure 3. Transitions between adjacent bus wires

The above coding scheme adds two extra lines (code bits) to the bus. The value on the bus  $L(k)$  at time instant “k” can now be represented as:

$$L(k) = \{L_D(k), L_C(k)\}$$

where  $L_D(k)$  and  $L_C(k)$  represent the data bit part and the code bit part respectively.

### 3. Encoding Hardware

The encoding hardware consists of four modules as shown in Figure 4. They are:

(i) Coupling Transition Estimator

The coupling transition estimator consists of an estimator and an adder stage. The estimator calculates the coupling transitions. The newly arrived data is compared with the immediate past data on the bus and the number of transitions  $s_i(k)$  and  $r_i(k)$  for each pair of bus wires is calculated. The adders then accumulate  $s_i(k)$  and  $r_i(k)$  for the whole bus to generate the total number of coupling transitions  $Q(k)$ .

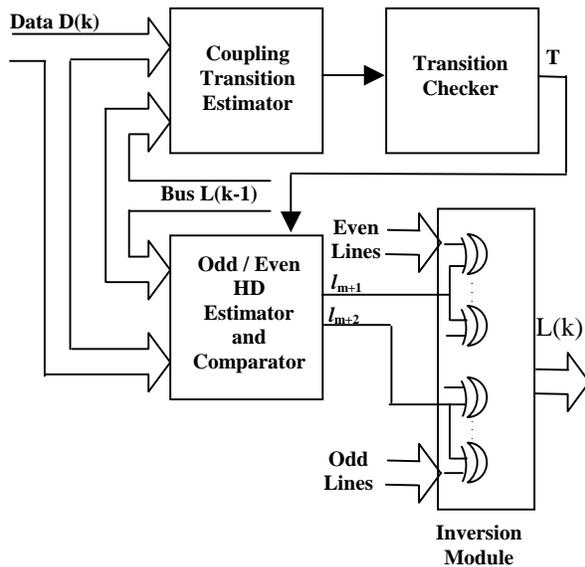


Figure 4. Encoding Hardware

(ii) Transition Checker

The transition checker checks whether  $Q(k) > m/2$ . If  $Q(k)$  is greater, then it produces a logic '1' at its output 'T', else a logic '0'.

(iii) Odd / Even HD Estimator and Comparator

This module separately calculates the HD between the present state and the next state on the even bus lines and the odd bus lines, and generates two logic signals EV and OD to indicate the relative magnitudes of the two

values, as given in Table 2. A combinational logic circuit then generates the two outputs  $l_{m+1}(k)$  and  $l_{m+2}(k)$  using the following Boolean relations:

$$l_{m+1}(k) = T \overline{OD} \text{ and}$$

$$l_{m+2}(k) = T \overline{EV}$$

The above two outputs form the code bit part of the bus  $L_C(k) = \{l_{m+1}(k), l_{m+2}(k)\}$  and are transmitted on the extra bus wires of the bus.

Table 2. Odd/Even HD estimator and comparator

EV	OD	
0	0	Equal HD
0	1	HD on odd lines greater
1	0	HD on even lines greater
1	1	Undefined

(iv) Inversion Module

This module decides how the data will be transmitted on the bus. If the Transition checker output T is zero, then the new data is transmitted as is. Else, the data will be inverted and transmitted accordingly to Table 3. The code bits  $L_C(k) = \{l_{m+1}(k), l_{m+2}(k)\}$  control this module.

Table 3. Coding of extra bus lines

$l_{m+2}(k)$	$l_{m+1}(k)$	Bus Inverted
0	0	No inversion
0	1	Even Lines
1	0	Odd Lines
1	1	Both Even and Odd lines

Hence this module consists of a set of Exclusive-OR (XOR) gates controlled by the code bits  $l_{m+1}$  and  $l_{m+2}$ .

### 4. An Illustrative Example

To illustrate our coding scheme consider a 16 bit data (1100,0010,1000,0111), which is

presently on the bus. If the next data (1010,1001,0011,0101) is sent as is, we have a total of  $14\lambda$  coupling transitions ( $Q(k)$ ). Since  $Q(k)$  is more than half the word length (8), the data will be encoded using our method. In this case, the number of transitions on odd lines of the bus (6) exceeds that on the even lines (3). (In determining the odd/even lines, the least significant bit is counted as number zero.) So the odd bits of the data are inverted (even bits stay the same) and sent through the bus with the additional two lines appended (10,0000,0011,1001,1111). The additional two bits are appended so that the decoder can decode accordingly as specified in Table 3. For this example it may be noted that  $R(k) = 6$  while  $S(k) = 8$ . By applying our coding scheme we have reduced new  $R(k)$  to 0 and  $S(k)$  to 2. The total number of transitions  $Q(k)$  for unencoded and encoded data are 14 and 2 respectively. Hence, we see that the total number of coupling transitions is reduced from  $14\lambda$  to  $2\lambda$ , thereby reducing the power consumption.

## 5. Performance Evaluation

We have evaluated the effectiveness of our coding scheme using a MATLAB program. The simulations used 8 and 16 bit random data with 1000 data vectors. Figure 5 shows 8 bit simulation results using our technique.

The reduction in the number of transitions achieved is very close to that in the original bus invert coding technique, that took into account only self-transitions, whereas our method considered coupling transitions, which is a dominant factor in deep sub-micron buses. Simulation results show that about 10% reduction in coupling transitions is achieved by our technique.

## 6. Conclusions

We proposed a new coupling driven data encoding scheme for low power data transmission in deep sub-micron buses. The simulation results show that our technique reduces 10% of the coupling transitions for a deep sub-micron bus compared to the

conventional non-coded data transmission. As this method is adaptive, it reduces signal transmission for all sorts of data streams.

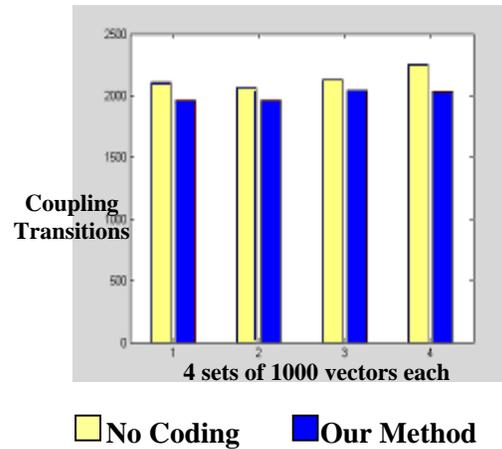


Figure 5. Coupling transitions for 8-bit data vectors

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