EGE534 HW #2 *Dr. Izadi*

Name: _____

Problem 1 (10 Points)
Design a one-bit 5MR voter using basic gates.

Problem 2 (20 Points)
A cyclic code is to be based on the Generator polynomial $X^7 + X^5 + X^4 + X^3 + 1$. Show the logic diagram for the code encoder.

a. Generate a codeword for the input data 10011.
b. Using logic gates, design an appropriate encoder and decoder the given cyclic code.

Problem 3 (20 Points)
A 2M X 16 memory system is design using 1 M X 4 chips. Assume chip failure modes are single-bit cell (55%), single-row all-0's (25%), single-column all-0's (15%), and whole-chip all-0's (5%). Also, assume 0 and 1 values are equally likely. Compare and comment on relative performance (single-error-detection coverage) and overhead of the following approaches.

a. Bit per chip
b. Bit per multiple chips
c. Duplication
d. Single precision checksum (one sum for the entire memory).

Problem 4 (10 Points)

a. Draw a block diagram showing the overall structure of a reconfigurable NMR system (i.e. N-modular redundancy with spares) based on hybrid redundancy. Briefly explain how the system tolerates fault.
b. Compare and contrast hybrid redundancy with active redundancy scheme. Discuss the main advantages and disadvantages of the two methods.

Problem 5 (20 Points)
Consider a low-cost residue code based on module 7.

a. Show how do you obtain residue-7 check bits of $X_7\ X_6\ X_5\ X_4\ X_3\ X_2\ X_1\ X_0$ using recursive addition technique?
b. What is the theoretical base for this easy encoding process? Hint: use the weights of bit groups.

Problem 6 (10 Points)
Convert 0 to 14 to RNS using modules [3,5,7]. Within this range would you say a single fault is detectable or not. Justify your answer

Problem 7 (20 Points)

a. Using full adders and basic gates, design a 3N code encoder, where N is a 4-bit binary number.
b. Design a circuit to detect an error in the above 3N code.

Due September 20, 2007