EGE 534 HW #2 Dr. Izadi

First Name:_____ Last Name: _____

*In doing your homework, please make sure you follow the following guidelines. Failure to follow them, will result in 0 grade:*

- *Only write on one side of your paper.*
- *Problem solutions must follow in order i.e. Start with Problem 1, then Problem 2 and etc. The solutions to each section must also be in order.*
- *Unless explicitly specified, you should not explain your solution – just provide your solution.*
- *Make sure that the papers are stapled and your name is on the paper.* Make sure your name appears exactly as shown on your registration.

Problem 1 (10 Points)
Design a one-bit 5MR voter using basic gates.

Problem 2 (10 Points)
Is $F = AC + \overline{B}$ a self-dual circuit? If not, transform it with the additional input D.

Problem 3 (10 Points)
Is full adder a self-dual circuit? If not, transform it with the additional input D.

Problem 4 (20 Points)
A 4G X 16 memory system is design using 1 G X 4 chips. Assume chip failure modes are single-bit cell (40%), single-row all-0's (20%), single-column all-0's (25%), and whole-chip all-0's (15%). Also, assume 0 and 1 values are equally likely. Compare and comment on relative performance (single-error-detection coverage) and overhead of the following approaches.

a. Bit per chip
b. Bit per multiple chips
c. Duplication
d. Single precision checksum (one sum for the entire memory).

Problem 5 (10 Points)
Determine the code distance of the following Hamming Error Correcting Code. Moreover, comment on its ability to detect and/or correct bit errors.

| $c_2c_1c_0$ | **Bit in Error** |
|---|---|
| 0 0 0 | No Error |
| 0 0 1 | $P_0$ |
| 0 1 0 | $P_1$ |
| 0 1 1 | $d_0$ |
| 1 0 0 | $p_2$ |
| 1 0 1 | $d_1$ |
| 1 1 0 | $d_2$ |
| 1 1 1 | $d_3$ |

Problem 6 (30 Points)
Consider a random-access memory that has an 7-bit data.

a) Determine the H matrix such that the error code computed by your Single Error Correcting Hamming code specifies the bit position of the error.
b) Show a block diagram of your data bus, memory, and various stages of parity generation and error correction mechanism.
c) Design the detailed design of parity generation, syndrome generation and error correction circuitry using basic gates.
d) How you would modify the SEC code you have defined above in order to obtain an SEC/DED code.

Due 2/13/2015