EGE 534   HW #1   Dr. Izadi

First Name:_____   Last Name: _____

Problem 1 (10 Points)
Design a one-bit 5MR voter using basic gates.

Problem 2 (10 Points)
Is $F = A\overline{C} + B$ a self-dual circuit? If not, transform it with the additional input D.

Problem 3 (10 Points)
Is full adder a self-dual circuit? If not, transform it with the additional input D.

Problem 4 (20 Points)
A 4G X 16 memory system is design using 1 G X 4 chips. Assume chip failure modes are single-bit cell (45%), single-row all-0's (30%), single-column all-0's (15%), and whole-chip all-0's (10%). Also, assume 0 and 1 values are equally likely. Compare and comment on relative performance (single-error-detection coverage) and overhead of the following approaches.
a. Bit per chip
b. Bit per multiple chips
c. Duplication
d. Single precision checksum (one sum for the entire memory).

Problem 5 (10 Points)
Show that the code distance of a 4bit data with a single even parity is adequate to make it candidate for a single error detection.

Problem 6 (30 Points)

Consider a random-access memory that has an 7-bit data.

a) Determine the H matrix such that the error code computed by your Single Error Correcting Hamming code specifies the bit position of the error.

b) Show a block diagram of your data bus, memory, and various stages of parity generation and error correction mechanism.

c) Design the detailed design of parity generation, syndrome generation and error correction circuitry using basic gates.

d) How you would modify the SEC code you have defined above in order to obtain an SEC/DED code.

Due 2/28/2014