EGE 534 HW #1 Dr. Izadi

First Name:_____ Last Name: _____

Problem 1 (10 Points)
Design a one-bit 5MR voter using basic gates.

Problem 2 (20 Points)
A 4G X 16 memory system is design using 1 G X 4 chips. Assume chip failure modes are single-bit cell (45%), single-row all-0's (30%), single-column all-0's (15%), and whole-chip all-0's (10%). Also, assume 0 and 1 values are equally likely. Compare and comment on relative performance (single-error-detection coverage) and overhead of the following approaches.

a. Bit per chip
b. Bit per multiple chips
c. Duplication
d. Single precision checksum (one sum for the entire memory).

Problem 3 (10 Points)
Show that the code distance of a 5bit data with a single even parity is adequate to make it candidate for a single error detection.

Problem 4 (30 Points)
Consider a random-access memory that has a word format $X_4\, X_3\, X_2\, X_1\, X_0$ of size 5 bits. We can use Hamming code to correct any single bit in this memory.

a. Determine the H matrix such that Single Error Correcting Hamming code specifies the bit position of the error.
b. Show a block diagram of your data bus, memory, and various stages of parity generation and error correction mechanism.
c. Design the detailed design of parity generation, syndrome generation and error correction circuitry using basic gates.
d. Given the four syndromes s_i computed by your SEC Hamming code for single-bit errors affecting data bit x_i, $0 \le i \le 4$. Also give the error-free syndrome s^*.
e. Explain how you would modify the SEC code you have defined above in order to obtain an SEC/DED code.

Problem 5 (20 Points)
A cyclic code is to be based on the Generator polynomial $X^7 + X^6 + X^4 + X^2 + 1$.

a. Generate a codeword for the input data 10111.
b. Using logic gates, design an appropriate encoder and decoder the given generator.

Due 2/22/13