Fault-Tolerant Design of Digital Systems

EGE 534

Hardware Redundancy – Basic Approaches & Models

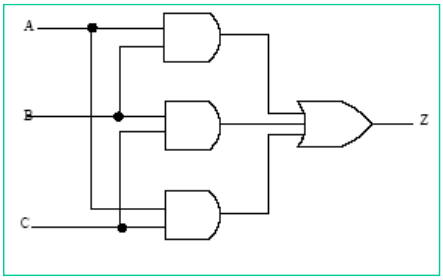
Dr. Baback Izadi
Division of Engineering Programs
State University of New York – New Paltz
bai@engr.newpaltz.edu

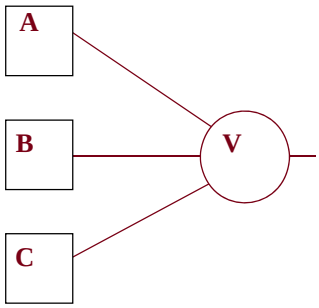
Basic Forms of Redundancy

- Fault-tolerance requires some form of redundancy
  - Hardware
  - Time
  - Software
- Hardware redundancy
  - Passive technique – Fault masking
  - Active technique – Dynamic method
  - Hybrid technique – Mix of two

Passive technique – Fault masking

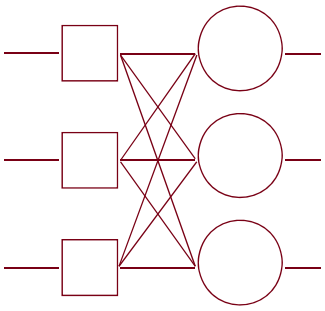
- Relies on voting to mask the occurrence of errors
- Can operate without need for error detection or system reconfiguration
- Triple modular redundancy (TMR)
- Design a one-bit voter

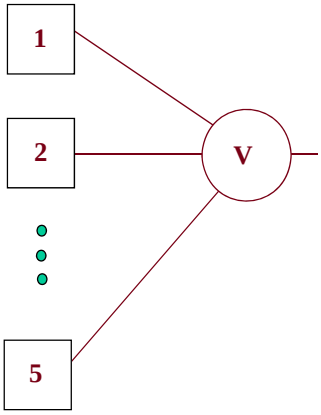




Passive technique – Fault masking

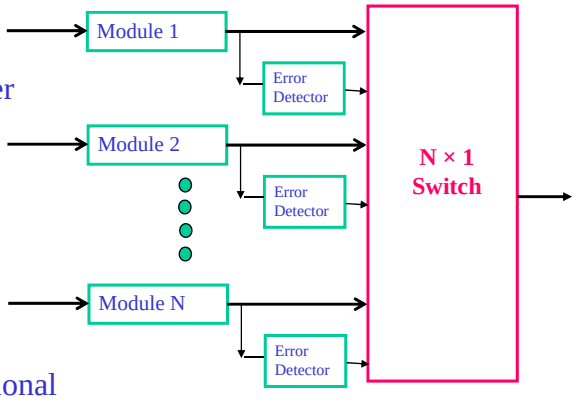
- 5MR tolerates 2 faulty unit
- N-modular redundancy (NMR)
  - Tolerates up to $\frac{N-1}{2}$ faults
- Voter single point of failure





Active Approach

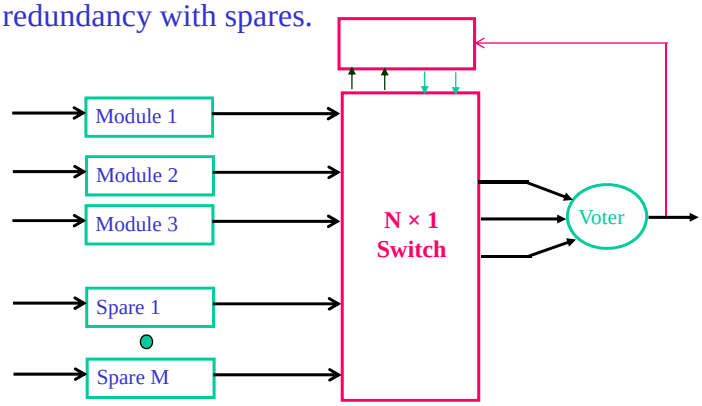
- Temporary erroneous result is accepted as long as the system reconfigures and regains its operation status within a set time.
- Achieves fault tolerance by
  - Error detection
    - Duplication
    - Watch dog timer
  - Fault location
  - Error recovery



- Standby sparing:
  - One module operational
  - One or more modules as spares

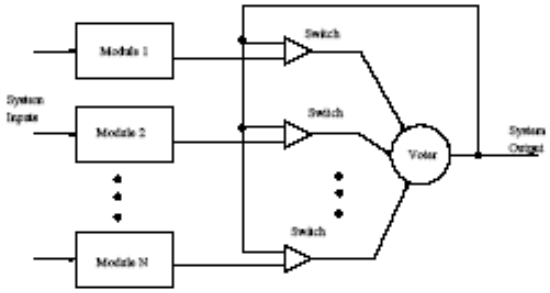
Hybrid redundancy

- Fault masking used to prevent system from producing erroneous results
- Fault detection, location, and recovery used to reconfigure system in event of an error.
- N-modular redundancy with spares.

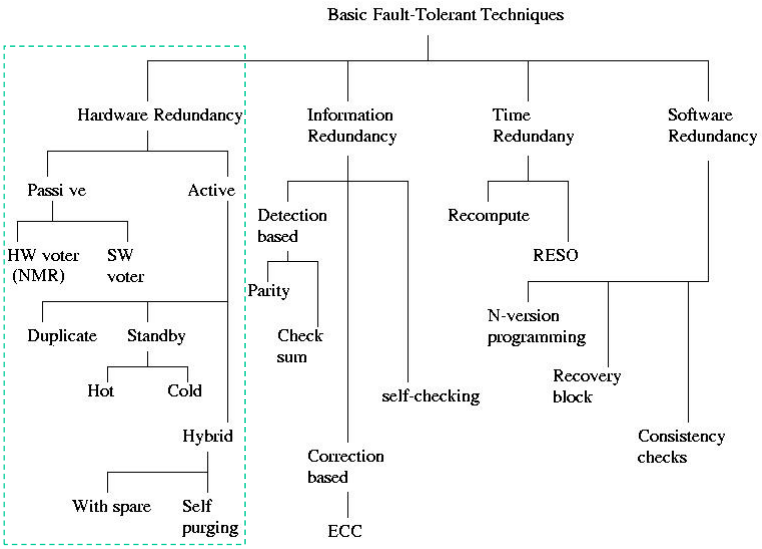


Self-Purging redundancy

- Similar to NMR with spares except that all units are actively participating in the system.
- Voter used is a **threshold gate**

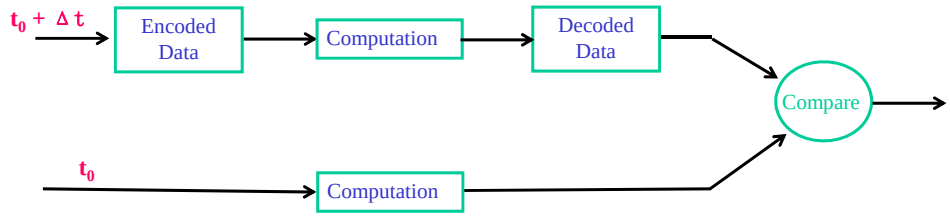


A summary chart of all techniques



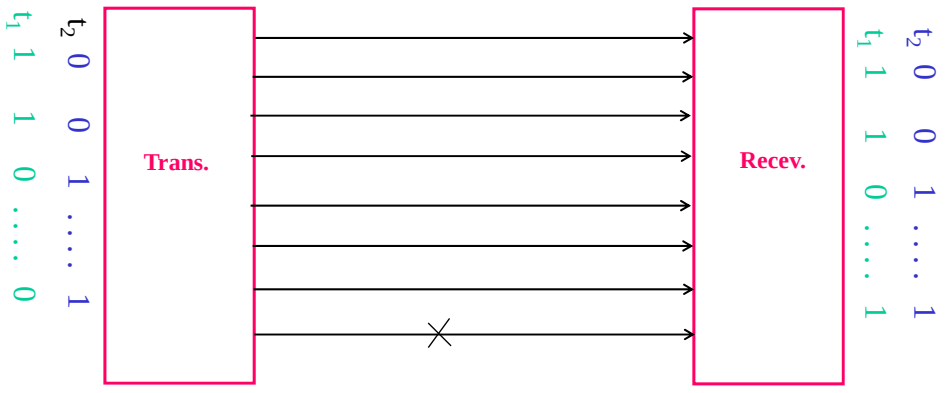
Time Redundancy

- Attempt to reduce the amount of extra hardware
  - In some applications, time is less important
- Transient Fault Detection
  - Perform the same computation multiple times and compare
- Permanent Fault Detection
  - Two computation is performed, one with the original data, the other with the encoded data



Time Redundancy – Alternative Logic

- At time t_1, use original data
- At time t_2 use complement of data



Self Dual Circuit

- Alternative logic is well suited for self-dual
  - $f(x) = \overline{f(\overline{x})}$ ➔ $\overline{f(x)} = f(\overline{x})$
- Any Combinational circuit with n input variables can be transformed into a self-dual with no more than n+1 inputs
  - $f_{sd}(x) = x_{n+1}f(x) + \overline{x_{n+1}}f_d(x)$
  - Where $f_d(x)$ is the dual of $f(x)$
- Example: $f = A\overline{B} + BC$
  - $f_d = (A + \overline{B})(B + C)$
  - $f_{sd} = D(A\overline{B} + BC) + \overline{D}(A+\overline{B})(B+C)$