New Paltz
STATE UNIVERSITY OF NEW YORK
Division of Engineering Programs

EGC442 Introduction to Computer Architecture

Test 1

First Name:____________ Last Name: _______________________

- You are allowed to print a copy of the instruction sheet.
  http://www.engr.newpaltz.edu/~bai/EGC442/Instructin%20set%20reference.pdf
- Your submission must be in a single PDF file
- Make sure you submit before the deadline of 1:45 PM. I will not accept late submission by email.
- You must adhere to the honor code. Any evidence of misconduct will be dealt with strictly per syllabus.

Question 1 (10 points)
Convert -12.75_{10} to single precision IEEE 754 format. Show your representation in binary.

8 4 2 1 .5 .25
1100.11 = 1.10011 x 2^3
exp = 127+3 = 130

| 1 | 1000 0010 | 10011000 - - - - - - - 0 |

Question 2 (10 points)
A program runs in 100 seconds. Multiply and divide operations are responsible for 30 and 40 of those seconds, respectively. Would it be possible to run the program 2 times faster?

3 a. By improving the multiplication alone. If yes, by what factor?
3 b. By improving the division alone. If yes, by what factor?
4 c. By improving the multiplication and division by the same factor. If yes, by what factor?

mult Divide other
100 = 30 + 40 + 30

2X

a. 50 ≠ + 70
not Possible

b. 50 = 60 +
not Possible

c. 50 = 20 + 30

$\frac{70}{20} = 3.5X$

Question 3 (15 points)

Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 200 ps and a CPI of 2.0 a program with 2×10^6 instructions, and computer B has a clock cycle time of 350 ps and a CPI of 1.2 for the same program.

3 a. How many clock cycles each computer execute?
4 b. What is the execution time of each processor?
4 c. What is the MIPS rating of each processor?
4 d. Which processor is a better processor? Why?

$T_A = 200 \times 10^{-12}$ $CPI_A = 2$ $N_A = 2 \times 10^6$

$T_B = 350 \times 10^{-12}$ $CPI_B = 1.2$

a. $CLK_A = 2 \times 10^6 \times 2 = 4 \times 10^6$

$CLK_B = 2 \times 10^6 \times 1.2 = 2.4 \times 10^6$

b. $Texe_A = 2 \times 10^6 \text{ instr} \times 2 \frac{clk}{instr} \times 200 \times 10^{-12} \frac{sec}{clk} = 800 \times 10^{-6} \text{ sec.}$

$Texe_B = 2 \times 10^6 \text{ instr} \times 1.2 \frac{CLK}{instr} \times 350 \times 10^{-12} \frac{sec}{CLK} = 840 \times 10^{-6} \text{ sec.}$

c. $MIPS_A = \frac{2 \times 10^6}{10^6 \times 800 \times 10^{-6}} = 2500$

$MIPS_B = \frac{2 \times 10^6}{10^6 \times 840 \times 10^{-6}} = 2381$

d. A is better due to lower execution time

Question 4 (15 points)
Replace the following C code by a set of equivalent MIPS instructions. Assume x, y, z, and i are in registers $t4, $t5, $t6, and $a2, respectively, and the staring address for array a is in register $s4.

```
if (x = = y)                 [x → $t4, y → $t5]
    a[i] = a[i] + a[i];      [a → $s4, i → $a2]
else
    a[i+1] = a[i] – z;       [z → $t6]
```

```
      sll   $a2, $a2, 2
      add   $s4, $s4, $a2
      lw    $t0, 0($s4)
      beq   $t4, $t5, else
      sub   $t0, $t0, $t6
      sw    $t0, 4($s4)
      J     out
ELES: add   $t0, $t0, $t0
      sw    $t0, 0($s4)
OUT:
```

0–5 small mistake
5–10 Med.
10–15 Big mistakes

Question 5 (10 points)
Assume $s3 has 5002, and words addressed 5000..5002 have the data shown:
5000: 0x99
5001: 0x77
5002: 0x23
5003:0x23
5004:0x6E
5005:0x34
5006:0x13
5007:0x34

a. What address will be computed by lw $t0, -2($s3) 0 X 5000
b. What value will be put in $t1 by lw $t1, 2($s3) → 5004

$t1 = 0 X 6E341334

Question 6 (15 points)
The following code segment is partially converted to machine code. Complete the conversion by placing appropriate values in the empty machine code fields of *sub, beq,* and *j* instructions.

			$t1	$a2	$t1		
Loop: sub $t1, $t1, $a2	0x58040000	0	9	6	9	0	0X22
lw $t0, 0($t1)	0x58040004	35	9	8	0		
beq $t0, $s5, Exit	0x58040008	4	8	21	2	(3)	
addi $s5, $s5, 1	0x5804000C	8	21	21	1		
j Loop	0x58040010	2	0X 1601 0000 (3)				
Exit: ...	0x58040014	xxxxxx					

0101 1000 0000 0100 0000 0000 0000 00|00

1 6 0 1 0 0 0 0

Question 7 (10 points)
Compare the number of gate delays for the critical paths of the following 32-bit adders

(2) i. Only using ripple carry
(4) ii. Using carry lookahead at the first level and ripple carry at between them
(4) iii. Using carry lookahead at the first and second level and ripple carry between second levels.

i. $32 \times 2 = 64$ gate delays

ii. $32/4 = 8$ modules

$8 \times 3 = 24$ gate delays

iii.

$\frac{32}{16} = 2$

$2 \times 5 = 10$ gate delays

Question 8 (15 points)
Show the internal architecture of the most significant bit of a 4-bit ALU as specified below.

$S_2S_1S_0$	Functions
000	AND (A ^ B)
001	XOR (A ⊕ B)
010	ADD (A + B)
110	Subtract (A - B)
111	SLT