EGC442 Quiz #24 Dr. Izadi

First NAME: Key Last Name: _____

1) Complete the following classification of computer systems.

		Instruction Streams	
		Single	**Multiple**
Data Streams	**Single**	SISD	SIMD
	Multiple	MISD	MIMD

2) According to Amdahl's law, what would the maximum speed up of a parallel system be with a code which 85% of it can be parallelized and remaining has to be executed sequentially, under

a. 10 processors
b. 100 processors
c. Infinite number of processors

Comment on what would an appropriate number of processors that should be dedicated to such a program?

$$S = \frac{1}{\beta + (1-\beta)/p}$$

a. $S = \frac{1}{0.15 + \frac{.85}{10}} = 4.26$

b. $S = \frac{1}{.15 + \frac{.85}{100}} = 6.31$

c. $S = \frac{1}{.15} = 6.67$

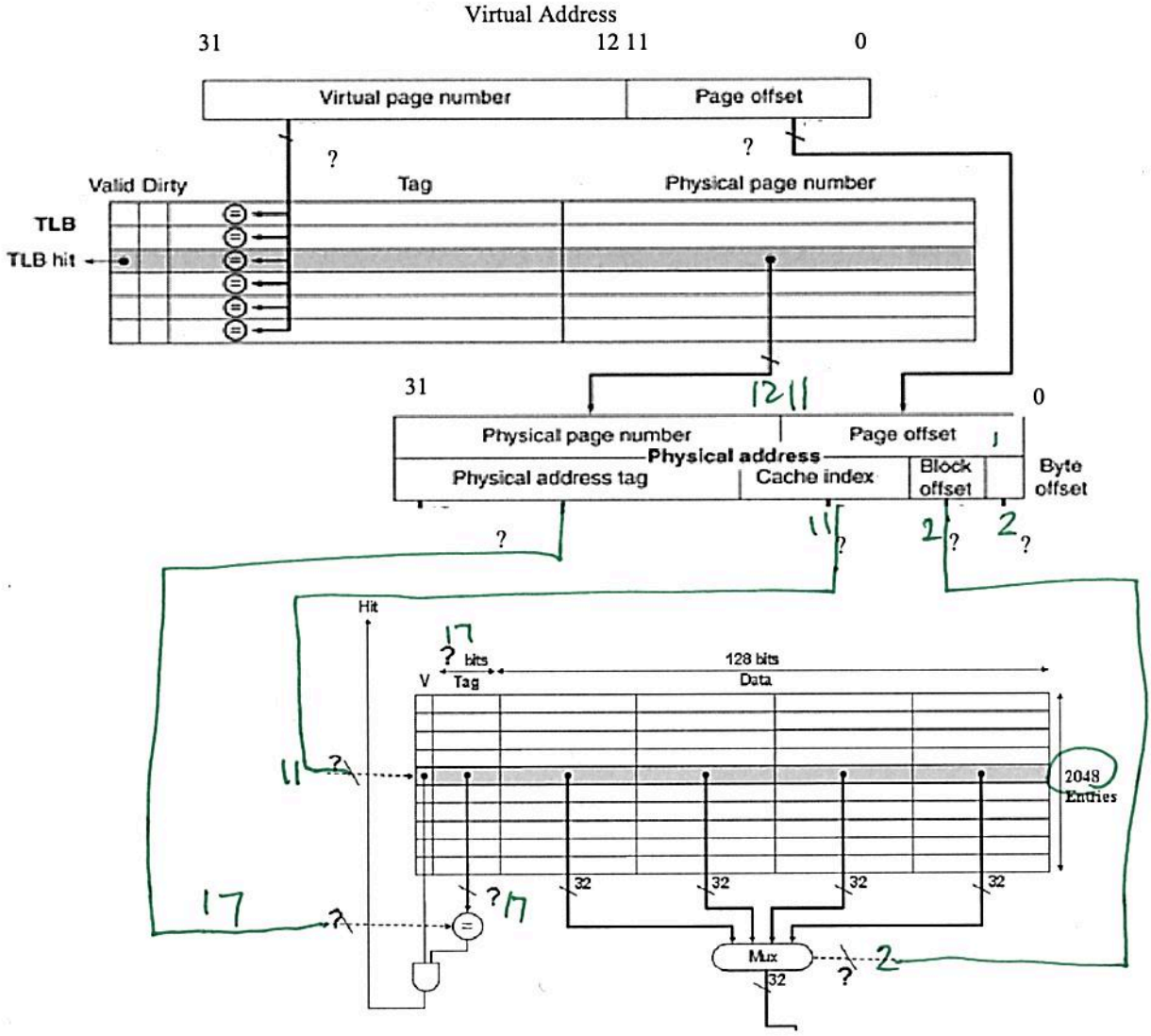
d. less than 100

EGC442 Quiz #23 *Dr. Izadi*

First NAME: Key Last Name: _____

The figure below depicts the memory system.

a. How many virtual pages numbers does the system have and how many bytes is each page? $2^{20} = 1M$
b. Identify type of cache architecture direct block size 4
c. Complete the cache architecture by connecting the dash lines to appropriate physical address.
d. Identify how many bits is each connection marked by "?".



EGC442 Quiz #22 Dr. Izadi

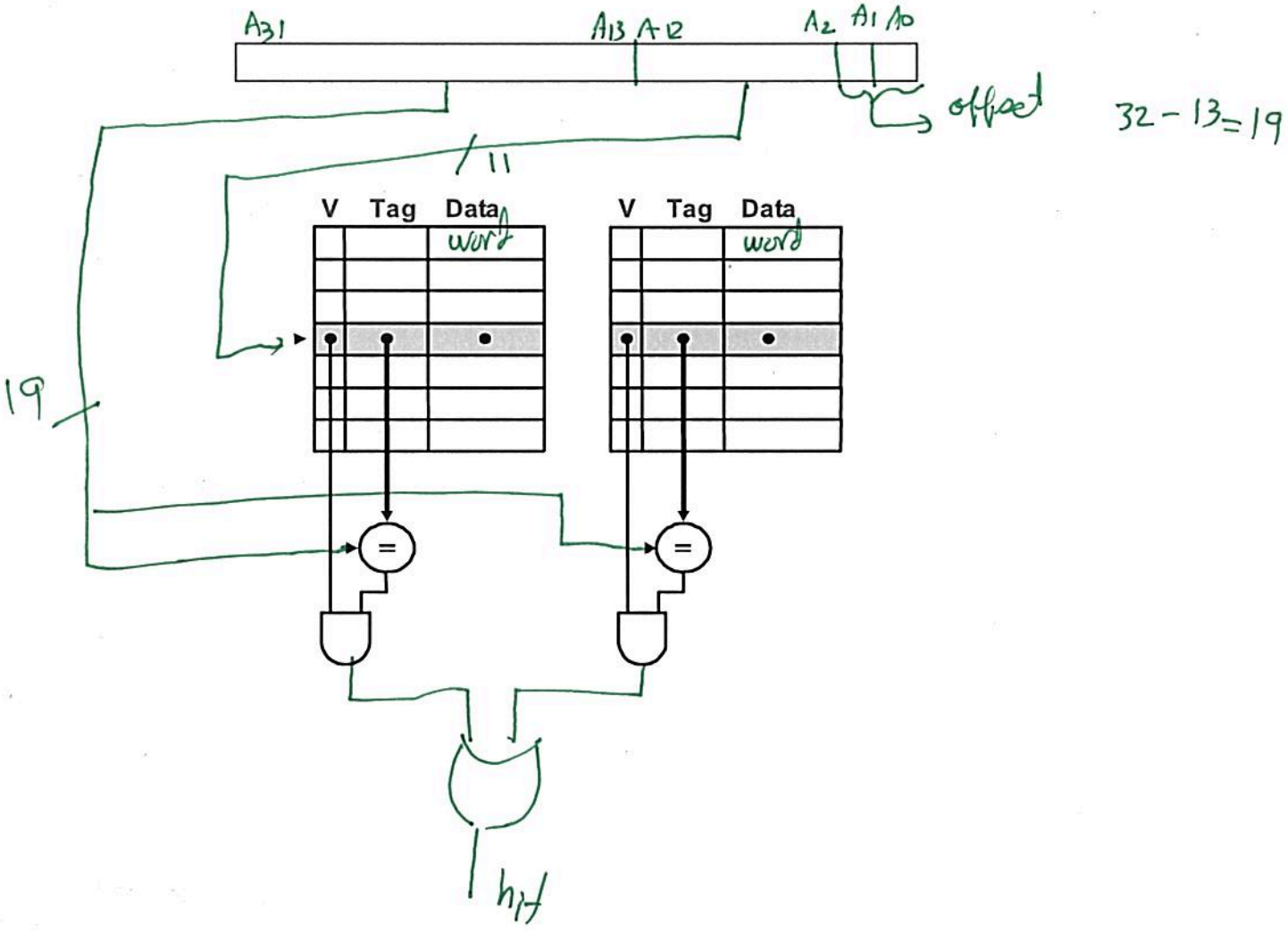
First NAME:_____ Last Name:_____

1) Design a 2 way set associative cache with the following parameters:

- Address size: 32 bits
- Cache size: 16 KB
- Word size: 4 Bytes

16K ÷ 4 = 4K ÷ 2 = 2K → 11 address index

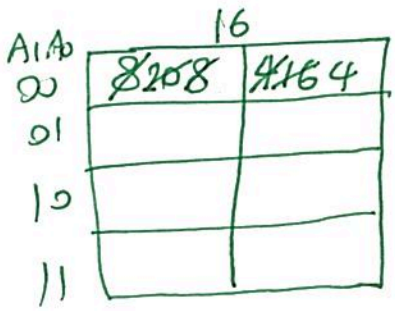
Complete the partially drawn diagram and indicate offset, index, and tag bits. Also, show the number of cache row entries.



2) The following is a series of address references given as word addresses: 8, 4, 20, 4, 16, 8, 4, 16, 4, 20, 4, 24. Assume two-way set associative cache with a word size of 1 byte and a total cache size of 8 bytes. Show the hits and misses and final cache contents and the final cache content. Assume FIFO (first in first out) replacement strategy.

1000
0100
10100
10000

Location	Hit/Miss?
8	M
4	M
20	M
4	H
16	M
8	M
4	M
16	M
4	H
20	M
4	M
24	M



3) Assume an instruction cache miss rate for an application is 1% and the data cache miss rate of 2%. Assume further that our CPU is running at 4 GHz and has a CPI of 2 without any memory stalls. The main memory access time is 50 ns. → 0.25ns

a. Determine the overall CPI with the indicated misses, provided the frequency of all loads and stores in the application is 30%.

b. Suppose we like to add a second level cache with an access time of 4 ns, which has an instruction miss rate of .4% and data cache miss rate of .6%. Determine the overall CPI.

$\frac{50ns}{.25ns} = 200$

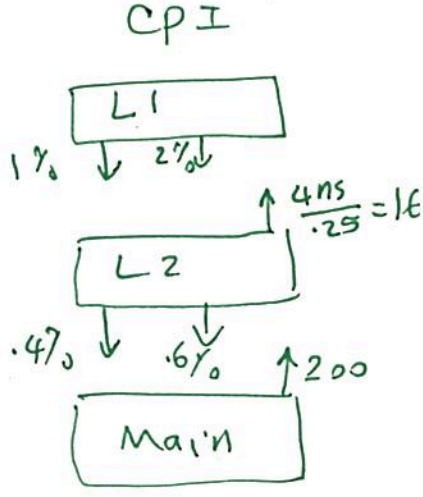
a. $CPI = 2 + 200 * .01 + 200 * .02 * .3$

$= 5.2$

b. $CPI = 2 + 16 * .01 + 16 * .02 * .3$

$+ 200 * .004 + 200 * .006 * .3$

$= 3.4$



EGC442 Quiz #21 Dr. Izadi

First NAME:_____ Last Name:_____

15 Points

1) Design a direct-mapped cache with the following parameters:

- Address size: 32 bits
- Total cache size: 16 KB
- Cache block: 4 word = 16 bytes

$\frac{16KB}{16} = 1K \rightarrow 2^{10}$

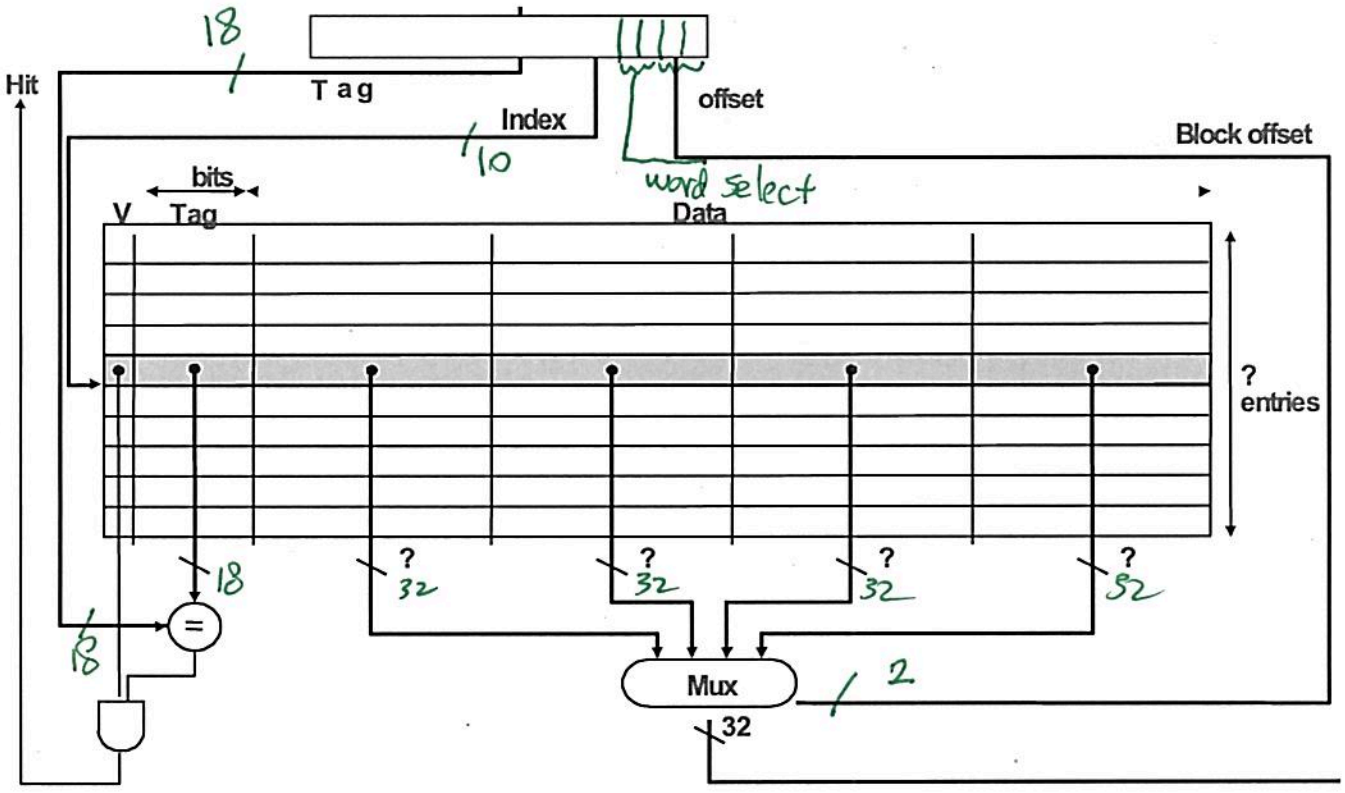
Indicate bit values for

a. Offset $2 + 2 = 4$

b. Index 10

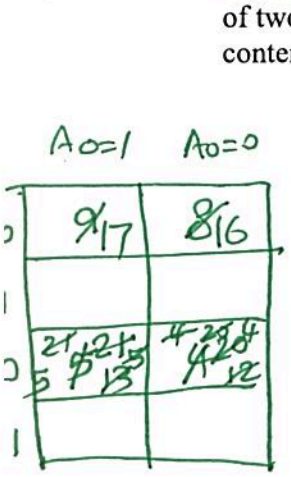
c. Tag 18

d. The number of cache row entries 1024



20 Points

2) The following is a series of address references given as word addresses: ~~5, 4, 20, 4, 21, 15, 5, 19, 4, 20, 4, 22~~. Assume direct map with a word size of 1 byte and a block size of two bytes and a total cache size of 8 bytes. Show the hits and misses and final cache contents and the final cache content.



Location	Hit/Miss?
8	M
4	M
20	M
4	M
8	H
12	M
4	M
16	M
4	H
20	M
4	M
16	H

15 Points

3) Assume an instruction cache miss rate for an application is 4% and the data cache miss rate of 6%. Assume further that our CPU has a CPI of 2 without any memory stalls and the miss penalty is 25 cycles for all misses. Determine the overall CPI with the indicated misses, provided the frequency of all loads and stores in the application is 20%.

$$CPI = 2 + 4\% * 25 + 6\% \times 20\% * 25$$

$$= 2 + 1 + 0.3$$

$$= 3.3$$

EGC442 Quiz #20 Dr. *Izadi*

First NAME: Key Last Name: _____

15 Points

1.

Index	V	Tag
000	Y	01_{two}
001	N	
010	N	
011	Y	00_{two}
100	N	
101	Y	11_{two}
110	Y	00_{two}
111	N	

a. After a request to address 10100, is the cache request a hit or miss? Why?

miss V = 0

b. Which memory location does cache reference 110 belong? In none, specify.

00110 6

c. Which memory location does cache reference 010 belong? If none, specify/

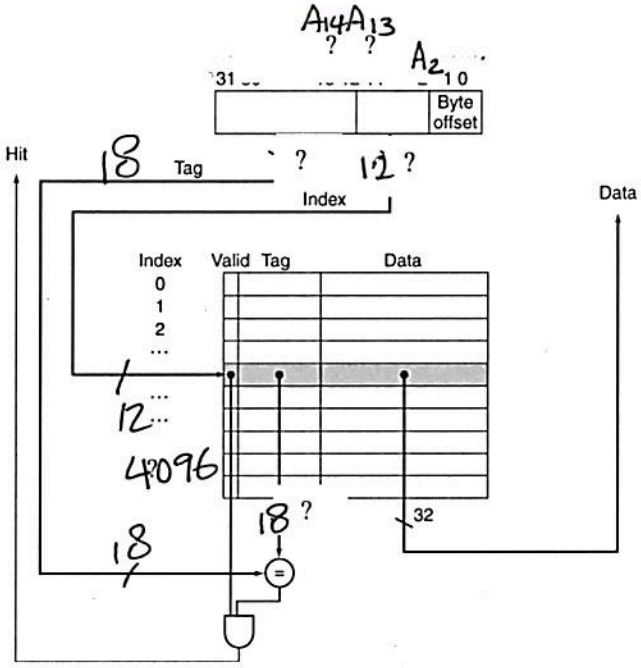
none

15 Points

2. Design a direct-mapped cache with the following parameters

- Address size: 32 bits
- Cache data size: 16 KB
- Cache block: 1 word

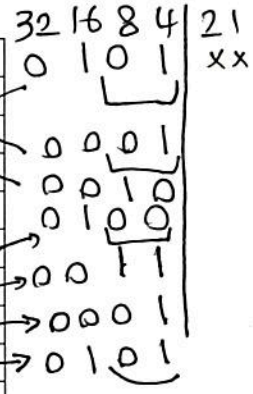
$16K \div 4 = 4K \rightarrow 2^{12}$



20 Points

3) The following is a series of address references given as word addresses: 20, 4, 8, 16, 8, 12, 4, 20, 4. Assume direct map with a word size of 4 bytes and a total size of 4 words. Show the hits and misses and final cache contents. Show the final cache content.

Location	Hit/Miss?
20	M
4	M
8	M
16	M
8	H
12	M
4	H
20	M
4	M



Index	Cache
00	16
01	20 4 20 4
10	8
11	12

EGC442 Quiz #19 *Dr. Izadi*

First NAME:_____ Last Name:_____

1) Given this instruction sequence,

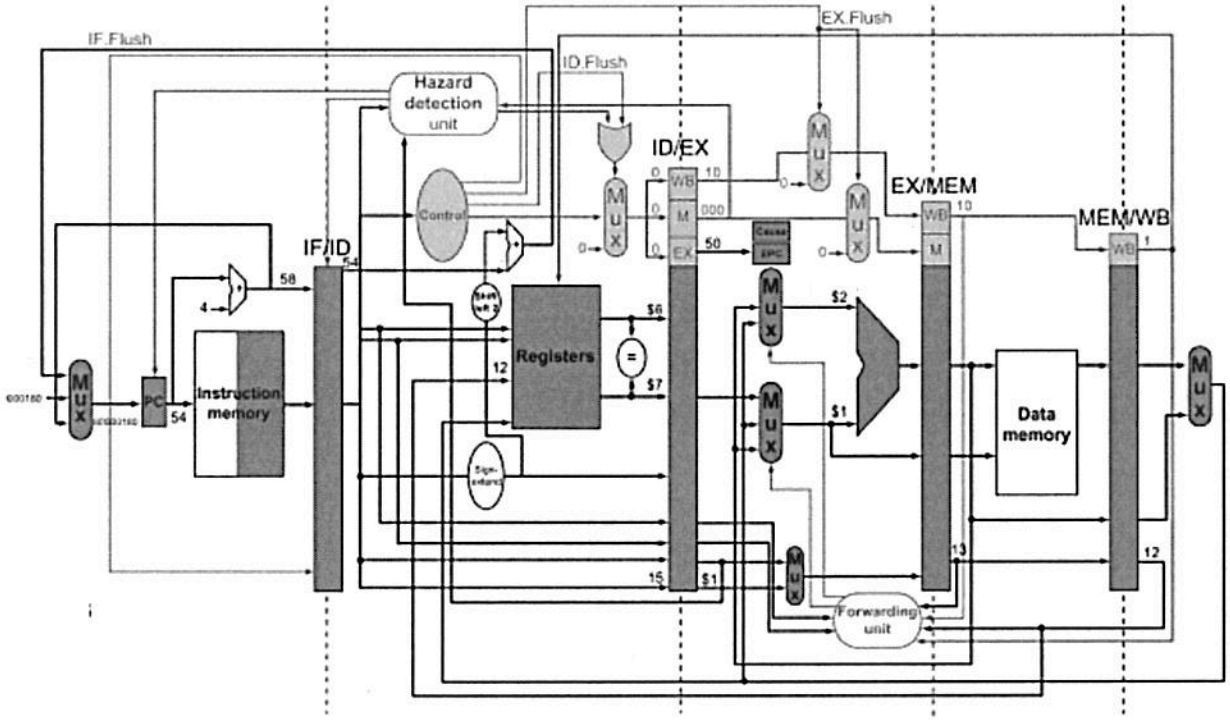
	40_{hex}	and	\$11, \$2, \$4
	44_{hex}	or	\$13, \$2, \$6
	48_{hex}	sub	\$12, \$2, \$4
→	$4C_{hex}$	add	\$1, \$2, \$1
	50_{hex}	slt	\$15, \$6, \$7
	$4C_{hex}$	lw	\$16, 50(\$7)
	…		

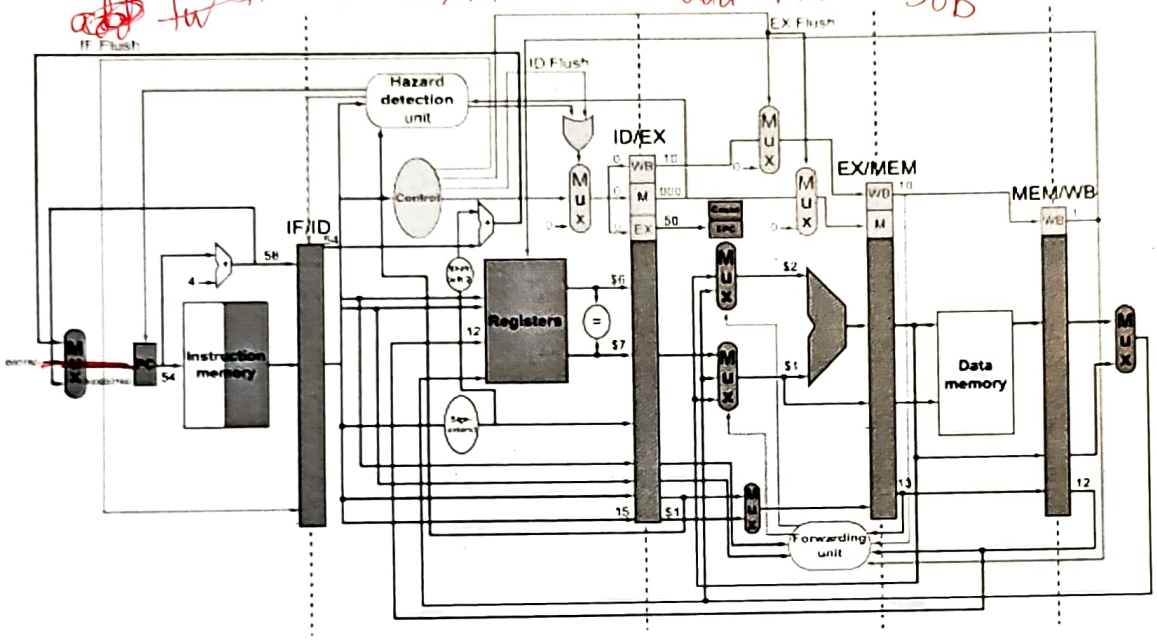
Assume the instructions to be invoked on an exception begin like this:

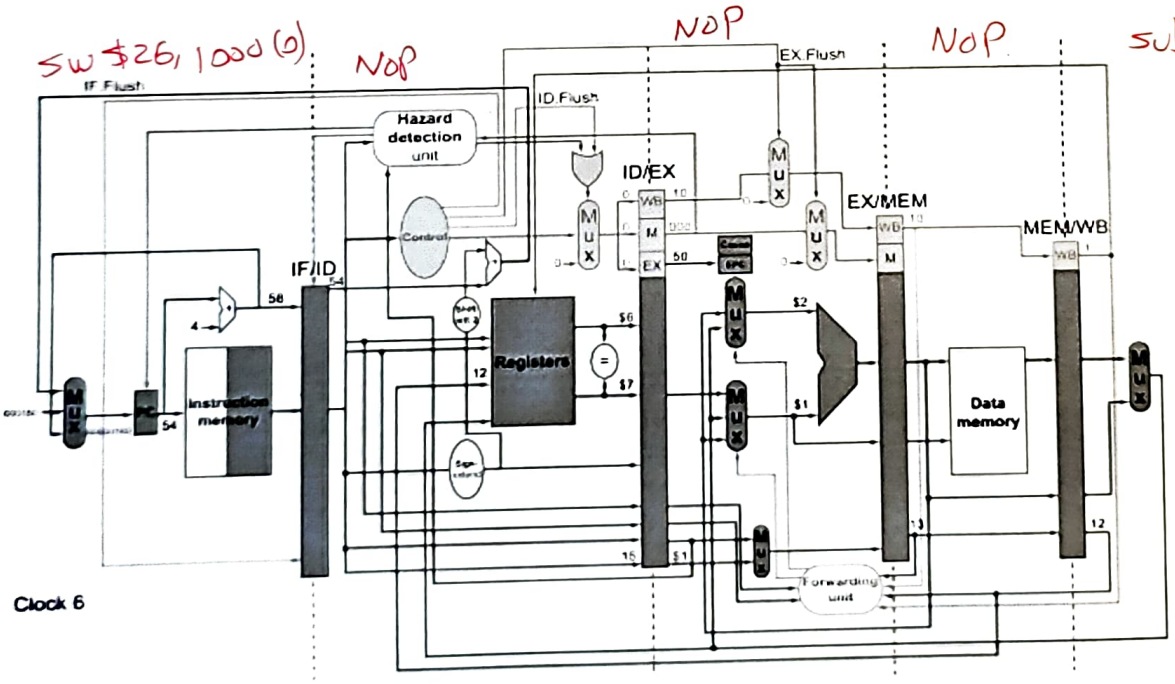
```
80000180hex   sw    $26, 1000($0)
80000184hex   sw    $27, 1004($0)
...
```

Show what happens in the pipeline if an overflow exception occurs in the ***add*** instruction.

slt \$15, \$6, \$7 add \$1, \$2, \$1 sub \$12, \$2, \$4




IF Flush
ID Flush
EX Flush
Hazard detection unit
Control
ID/EX
EX/MEM
MEM/WB
IF/ID
Registers
Instruction memory
Data memory
Forwarding unit
M u x
WB
M
EX


IF Flush
ID Flush
EX Flush
Hazard detection unit
Control
ID/EX
EX/MEM
MEM/WB
IF/ID
Registers
Instruction memory
Data memory
Forwarding unit
M u x
WB
M
EX
Clock 6

2) Show how the following loop can be scheduled on a static two-issue pipeline for MIPS?

```
up:  sub  $t0, $t0, $t0
     lw   $s1, 0($t1)
     sub  $s1, $s1, $a3
     sw   $s1, 0($t1)
     addi $t0, $t0, 1
     addi $t1, $t1, -8
     bne  $t1, $0, up
```

```
up:  sub  $t0, $t0, $t0
     lw   $s1, 0($t1)
     addi $t1, $t1, -8
     sub  $s1, $s1, $a3
     addi $t0, $t0, 1
     sw   $s1, 0($t1)
     bne  $t1, $0, up
```

Reorder the instructions to avoid as many pipeline stalls as possible without affecting the overall execution. Computer the overall IPC.

sub $t0,$t0,$t0	Nop
up: addi $t1,$t1,-8	lw $s1,0($t1)
sub $s1,$s1,$a3	Nop
addi $t0,$t0,1	sw $s1,0($t1)
bne $t1,$0,up	

$$IPC = \frac{7}{5} = 1.4$$

EGC442 Quiz #18 *Dr. Izadi*

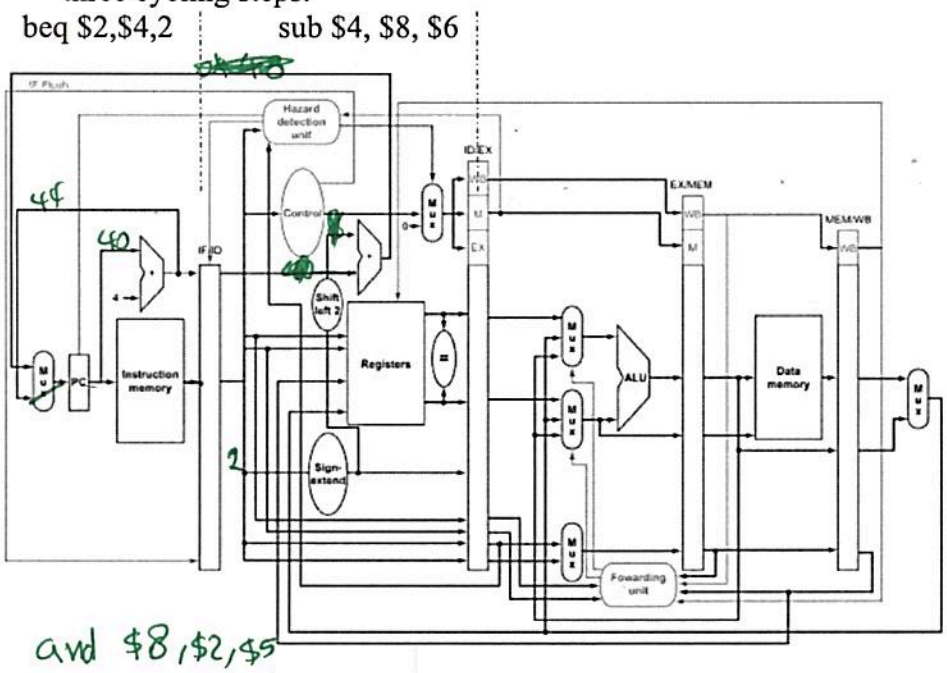
First NAME:_____ Last Name:_____

Assume the following sequence of instructions

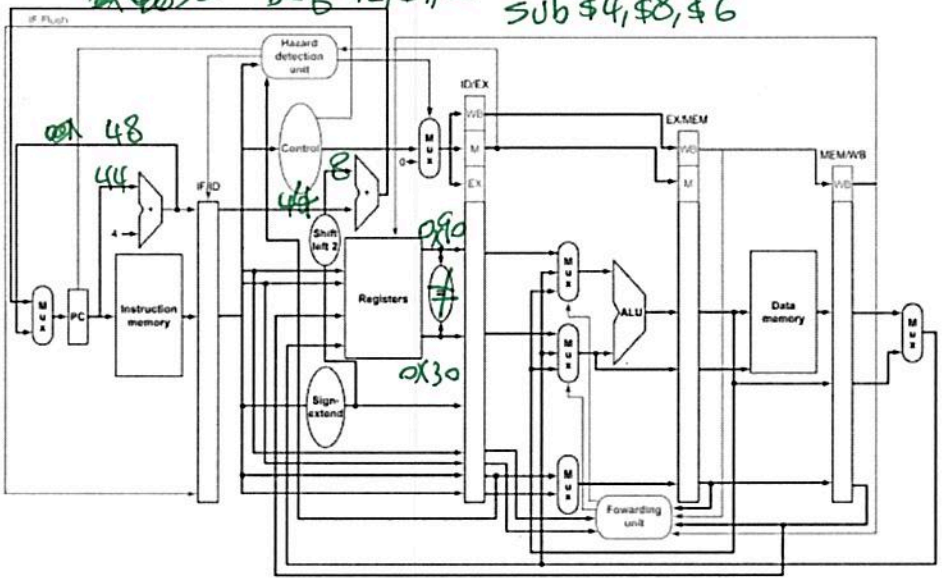
32 and $10, $4, $8
36 sub $4, $8, $6
40 beq $2, $4, 2
44 and $8, $2, $5
48 or $9, $2, $6
52 add $11, $4, $2
56 slt $15, $6, $7

a. Using the following diagram, assuming ($2)= 0x90 ($4)= 0x30, show the next three cycling steps:

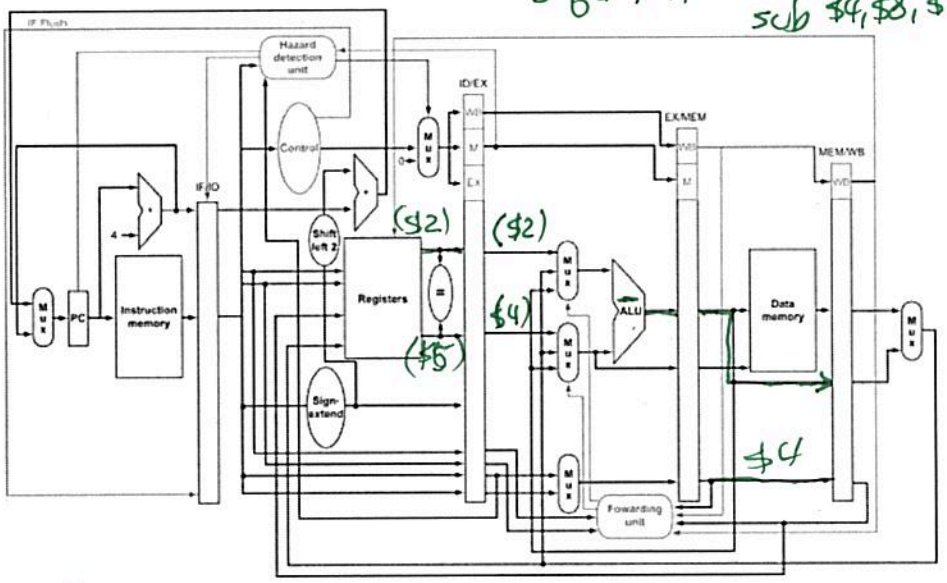
beq $2,$4,2 sub $4, $8, $6



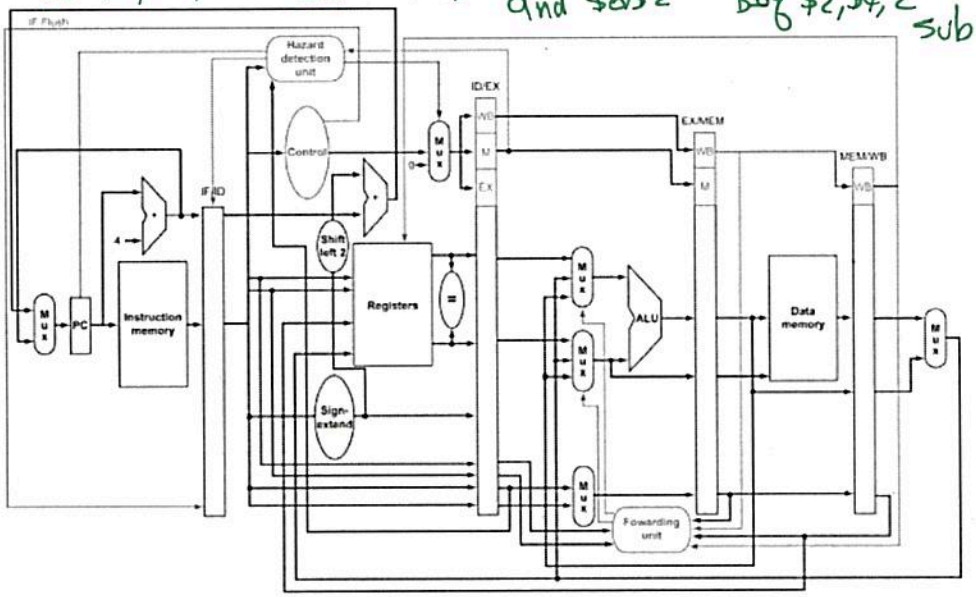
and $8,$2,$5 beq $2,$4,2 sub $4,$8,$6



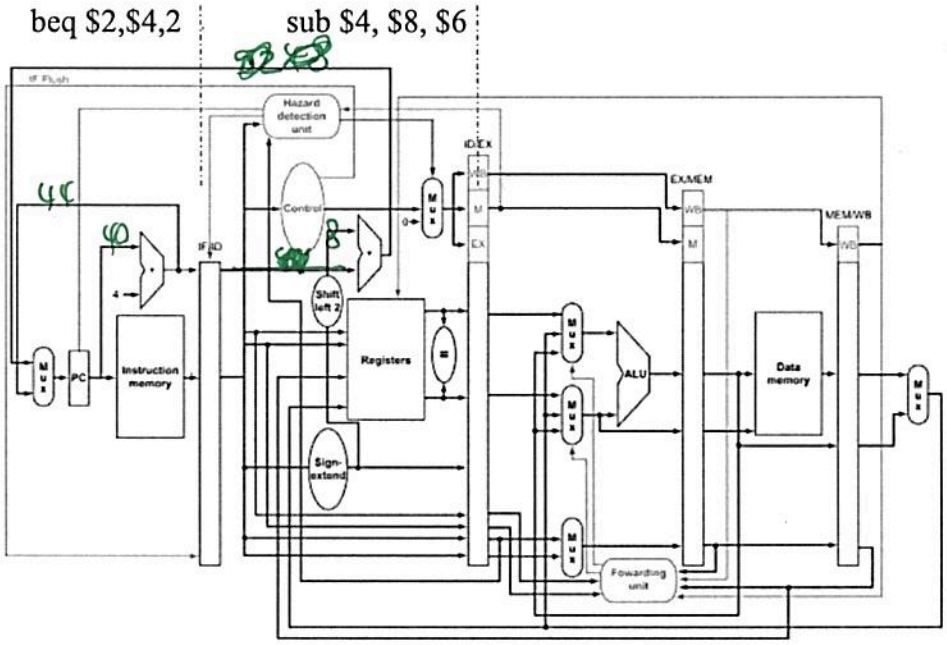
OR $9,$2,$6 and $8,$2,$5 Beq $2,$4,2 sub $4,$8,$6

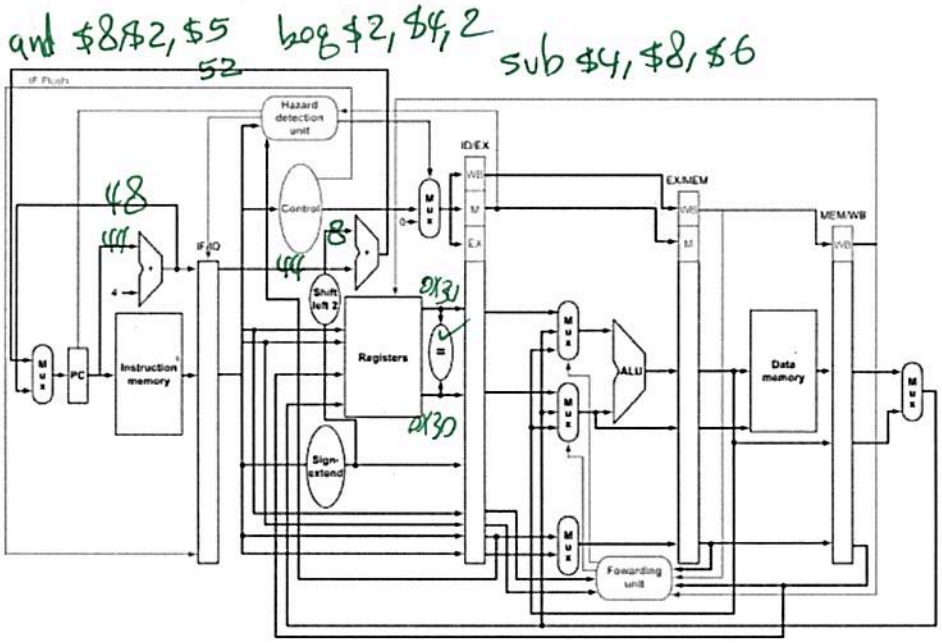


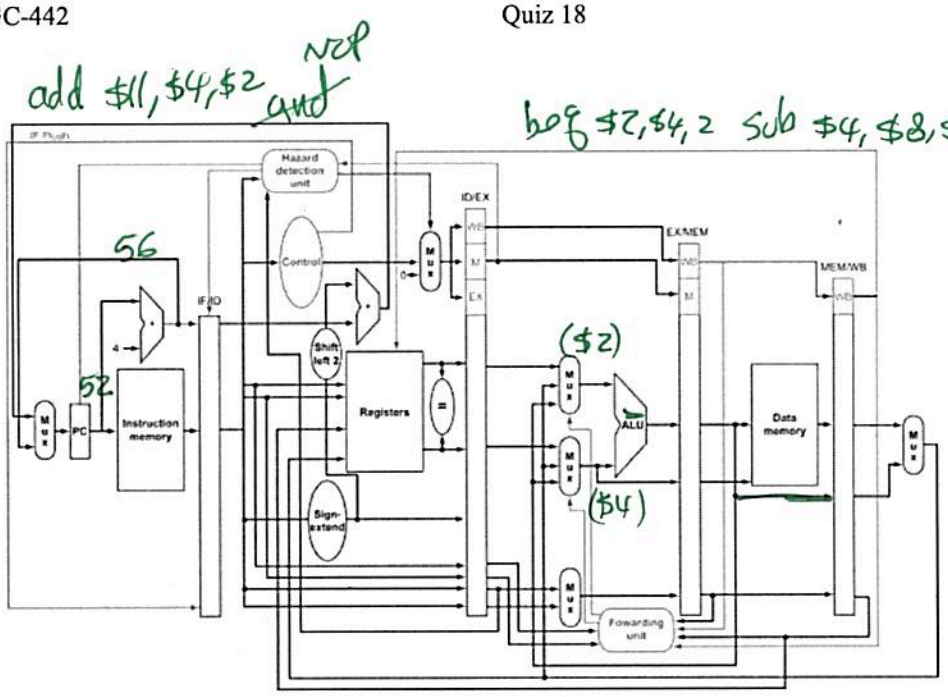
add $11,$4,$2 OR $9,$2,$6 and $8$2 Beq $2,$4,2 sub $4,$8,$6

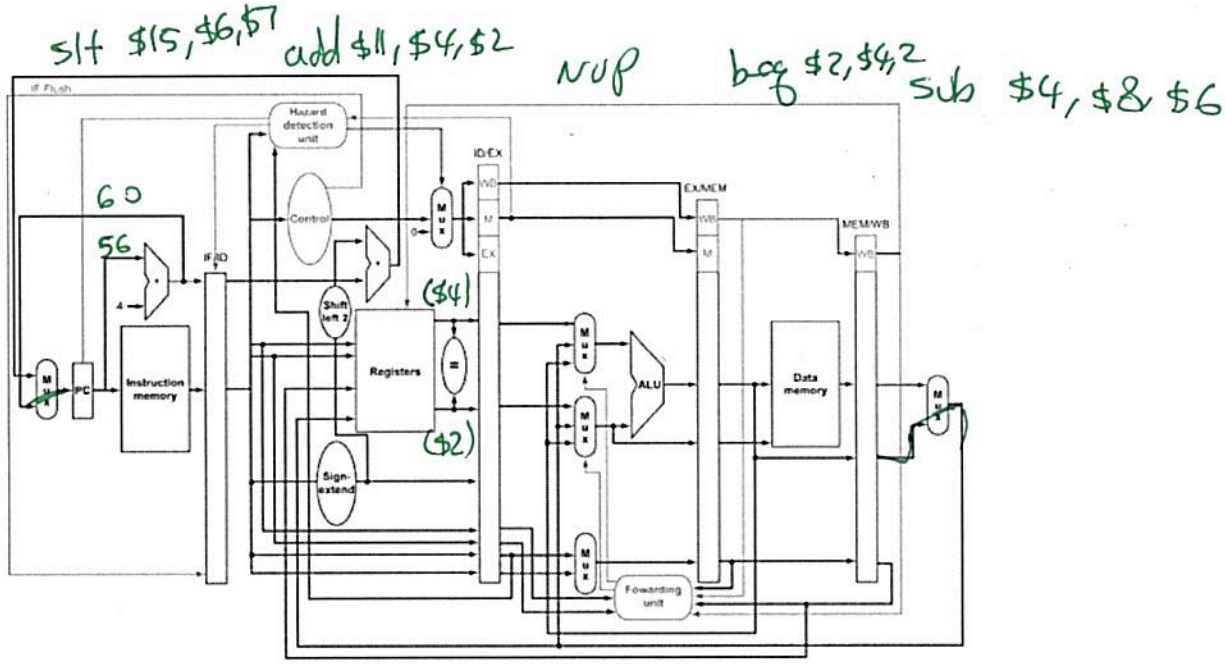


b. Repeat part a. for ($2)= 0x30 ($4)= 0x30






add $11, $4, $2
NOP
beq $2, $4, 2
sub $4, $8, $6
56
52
($2)
($4)
IF Flush
Hazard detection unit
Control
ID/EX
EX/MEM
MEM/WB
IF/ID
Shift left 2
Registers
Instruction memory
PC
ALU
Data memory
Sign-extend
Fowarding unit

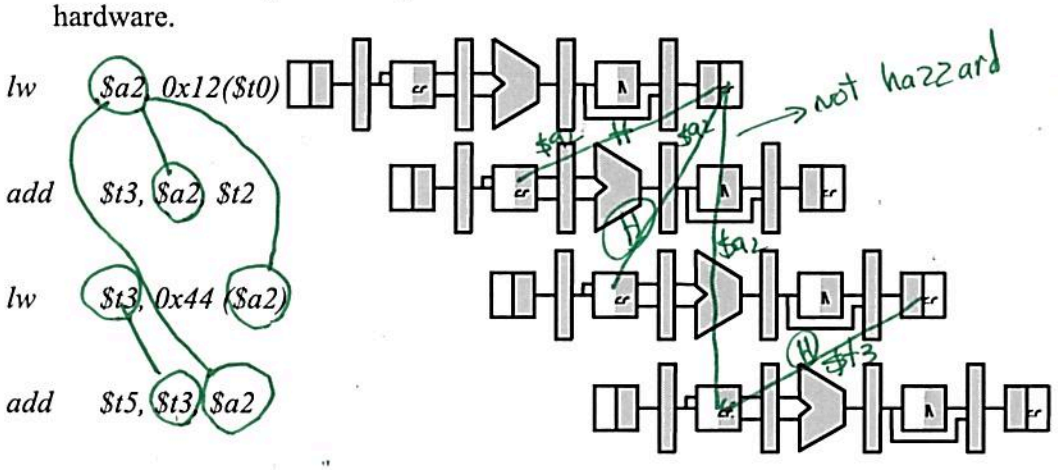

slt $15, $6, $7
add $11, $4, $2
NOP
beq $2, $4, 2
sub $4, $8, $6
60
56
($4)
($2)
IF Flush
Hazard detection unit
Control
ID/EX
EX/MEM
MEM/WB
IF/ID
Shift left 2
Registers
Instruction memory
PC
ALU
Data memory
Sign-extend
Fowarding unit

EGC442 Quiz #17 *Dr. Izadi*

First NAME:_____ Last Name:_____

For the code below,

a. On the diagram, mark and identify all the data dependencies in the code given below and identify which dependencies will cause data hazards without forwarding hardware.



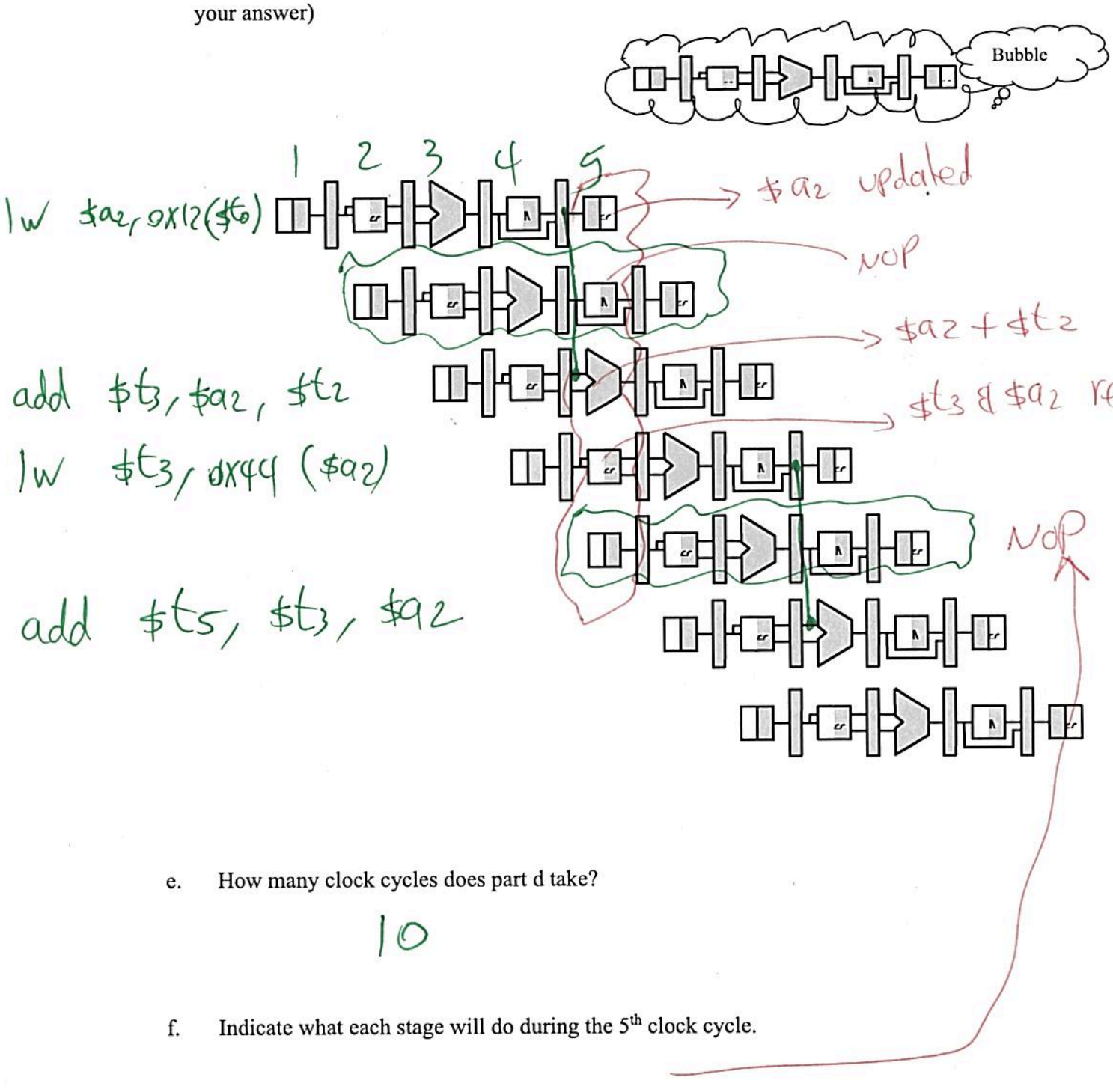
b. Assuming there is no special hardware that is added for forwarding. Add "nop" instructions to the code to avoid the data hazards.

```
lw   $a2, 0x12 ($t0)
nop
nop
nop
add  $t3, $a2, $t2
lw   $t3, 0x44 ($a2)
nop
nop
nop
add  $t5, $t3, $a2
```

c. How many clock cycles does it take to execute the code in part b.

14

d. Using forwarding, clearly show how it can be used to resolve data hazards. If a bubble needs to be added, simply make a marking as below. (use the next page for your answer)



e. How many clock cycles does part d take?

10

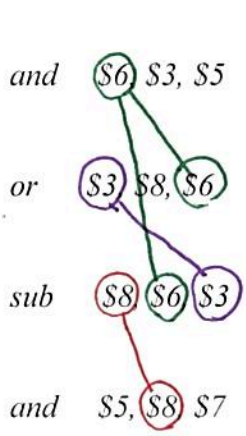
f. Indicate what each stage will do during the 5th clock cycle.

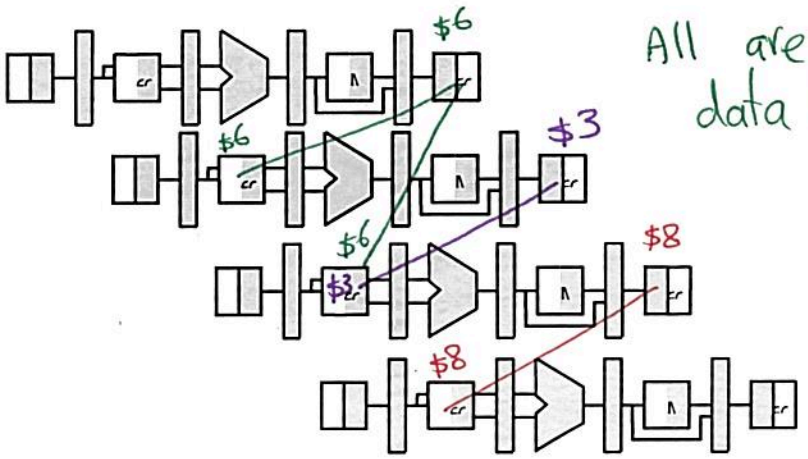
EGC442 Quiz #16 Dr. Izadi

First NAME:_____ Last Name:_____

For the code below,

a. On the diagram, mark and identify all the data dependencies in the code given below and identify which dependencies will cause data hazards without forwarding hardware.





All are data hazard

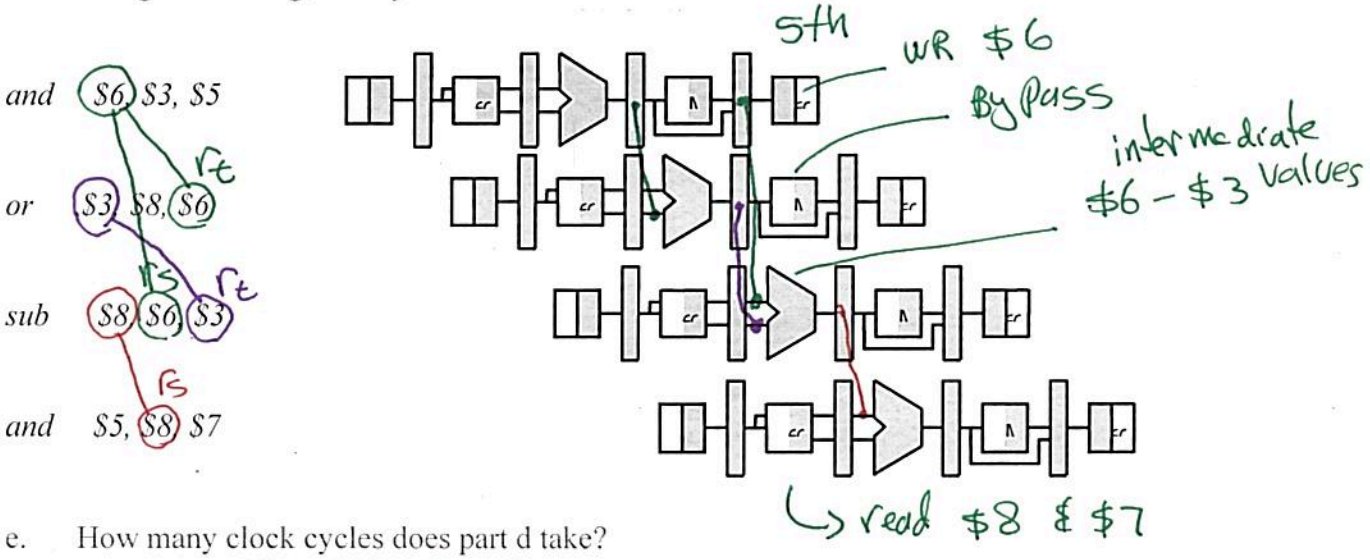
b. Assuming there is no special hardware that is added for forwarding. Add "nop" instructions to the code to avoid the data hazards.

```
and  $6, $3, $5
nop
nop
nop
or   $3, $8, $6
nop
nop
nop
sub  $8, $6, $3
nop
nop
nop
and  $5, $8, $7
```

c. How many clock cycles does it take to execute the code in part b.

17 CLK cycles

d. Using forwarding, clearly show how it can be used to resolve data hazards.



e. How many clock cycles does part d take?

8 clk cycles

f. Indicate what each stage will do during the 5th clock cycle.

Register write: WR $6

Memory: bypasss result of $8 or $6

ALU: subtract intermediate values $6 - $3

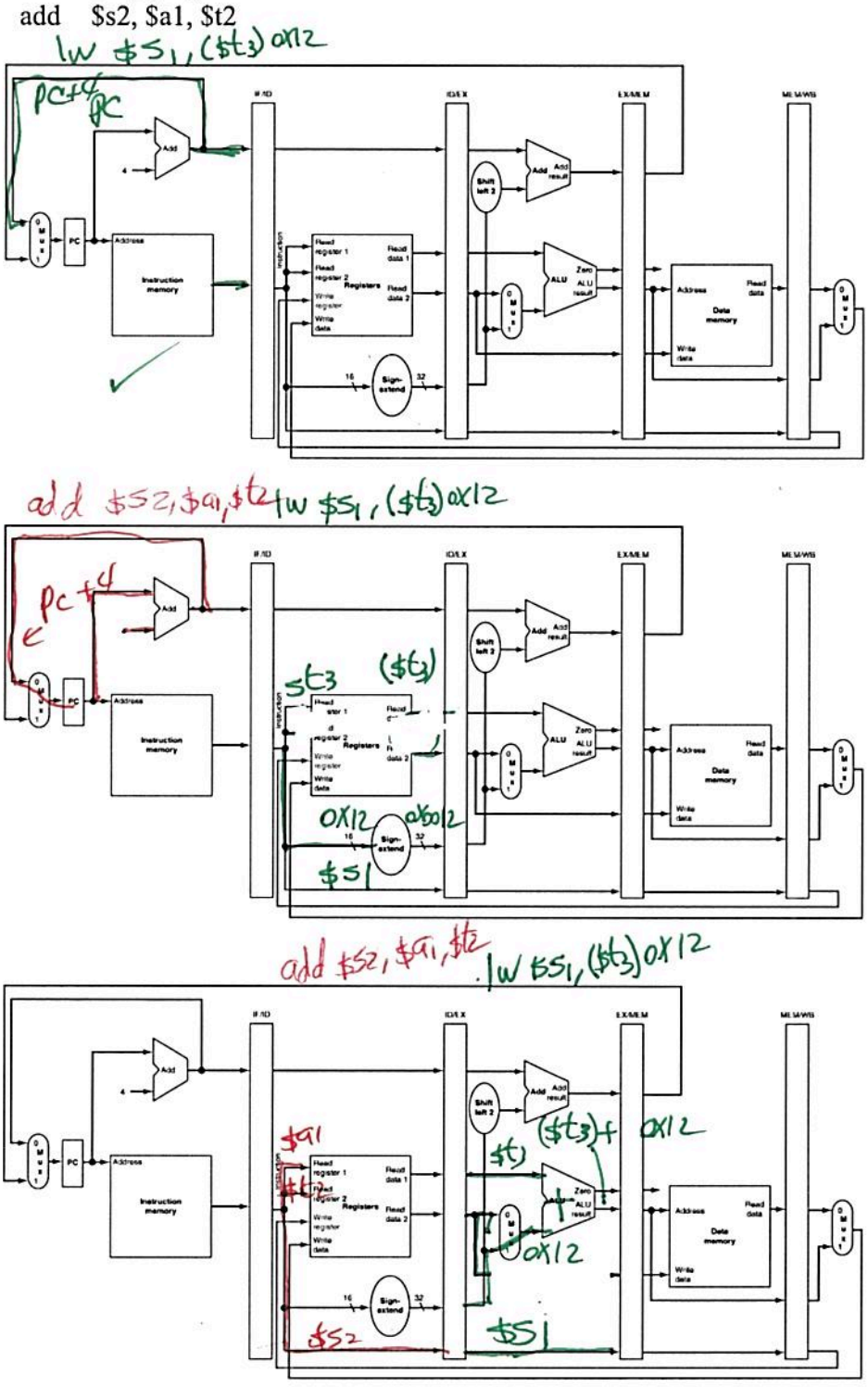
Register Read: read $8 & $7

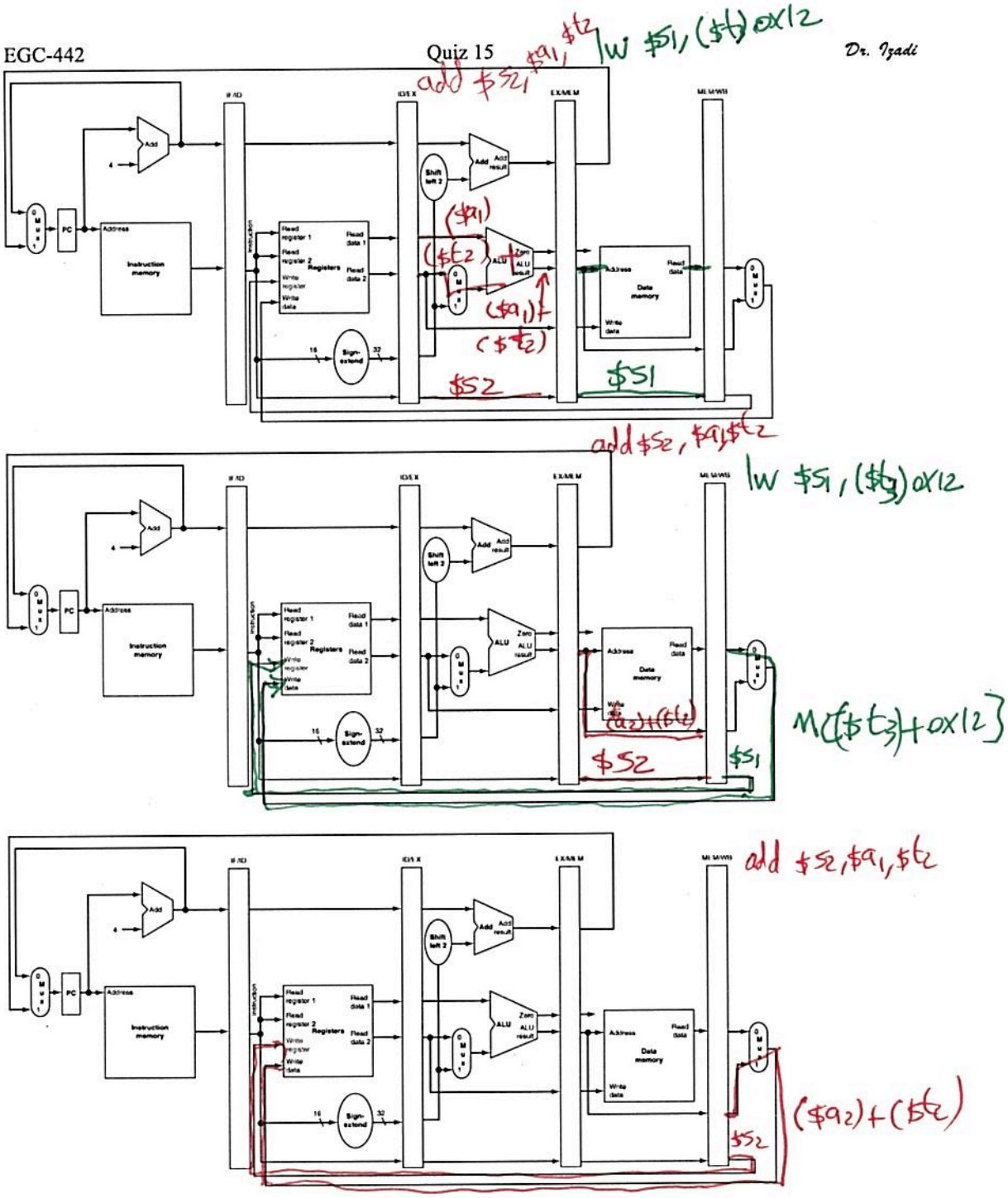
EGC442 Quiz #15 *Dr. Izadi*

First NAME:_____ Last Name:_____

Using multiple copies of the following diagram, show the active stages for execution of the following sequence of instruction set

lw $s1, ($t3)0x12
add $s2, $a1, $t2




add $s2, $s1, $t2
lw $s1, ($t3) ox12
($s1)
($t2)
($s1)+
($t2)
$s2
$s1
add $s2, $s1, $t2
lw $s1, ($t3) ox12
M{($t3)+ox12}
$s2
$s1
add $s2, $s1, $t2
($s1)+($t2)
$s2

EGC442 Quiz #14 Dr. *Izadi*

First NAME:_____ Last Name:_____

Problem 1 (25 Pt.)

a. Highlight and annotate the active data path with what they carry for:

beq $8, $9, 0x12

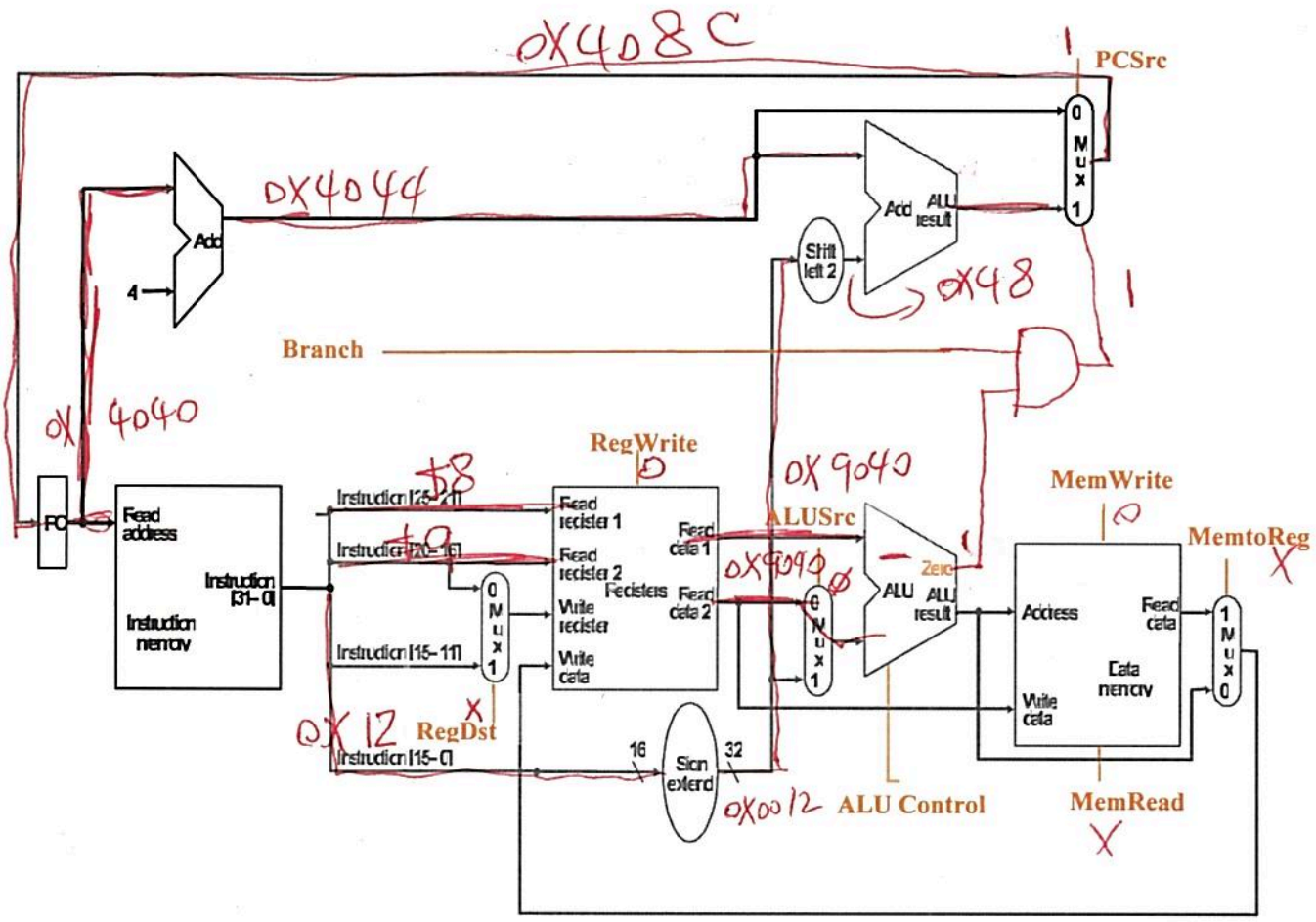
Assume prior to the execution, PC= 0X4040, $8 = 0X9040, $9= 0X9040.

b. Complete the control branch circuitry to allow beq to be executed and fill the following table with the associated control signal values:

Instruction	PCSrc	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUControl
beq	1	X	0	X	0	X	0	1	110

c. Determine the contents after the execution

$8 = 0x9040 $9= 0x9040 PC= 0X408C



Problem 2 (25 Pt.)

a. Highlight and annotate the active data path with what they carry for:

sw $2, 0x34 ($7)

Assume prior to the execution, PC= 0X4044, $2 = 0X9040, $7= 0X8480,
Mem[0x8480]= 0X 142A, Mem[0x8514] = 0X 3482, Mem[0x84B4]= 0x AC12

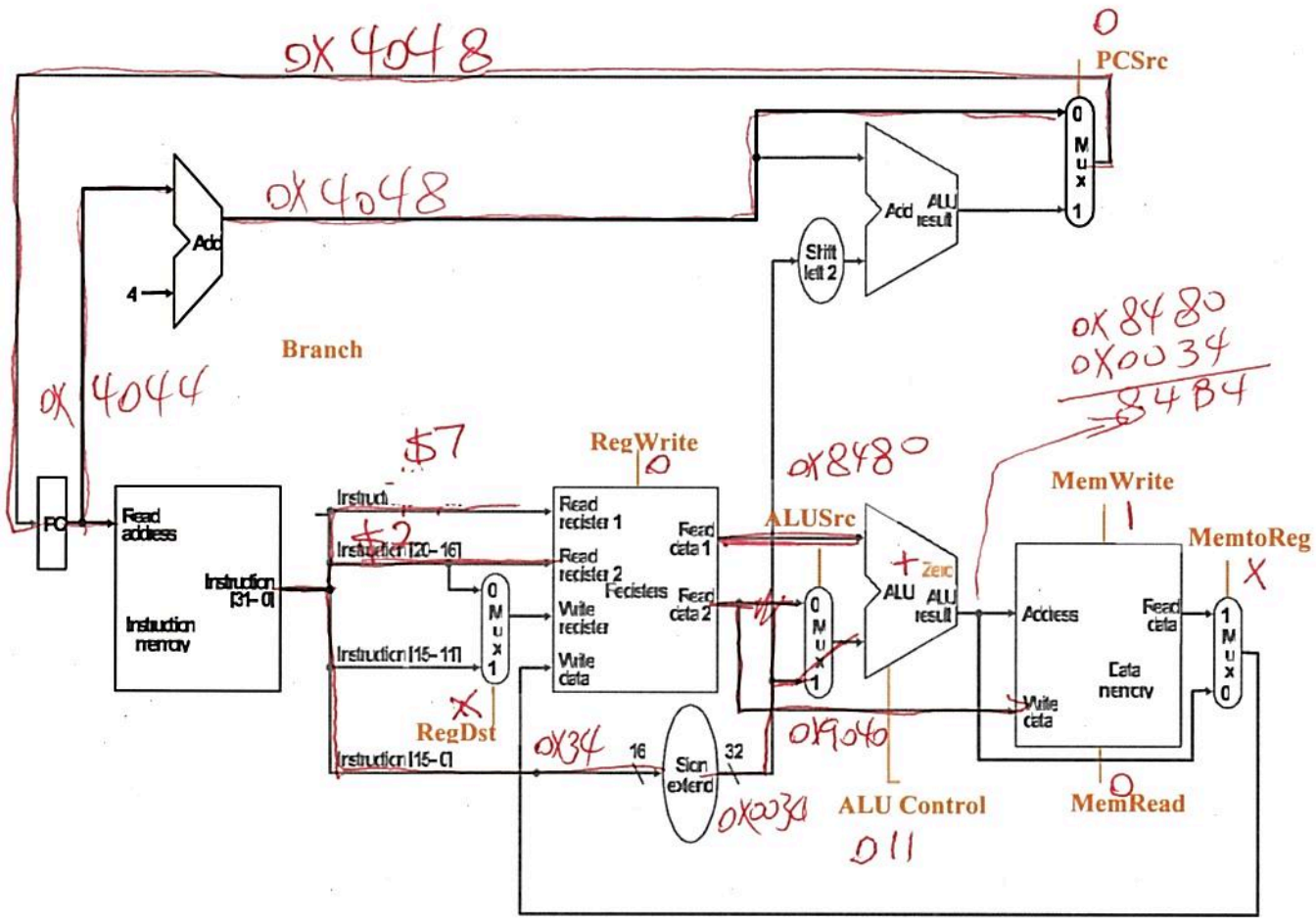
b. Fill the following table with the associated control signal values:

Instruction	PCSrc	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUControl
sw	0	X	1	X	0	0	1	0	010

c. Determine the contents after the execution

$2 =0X9040 $7=0X8480 Mem[0x8480]= 0X142A Mem[0x8514] = 0X 3482

Mem[0x84B4]= 0X9040 PC= 0X4048



EGC442 Quiz #13 *Dr. Iqadi*

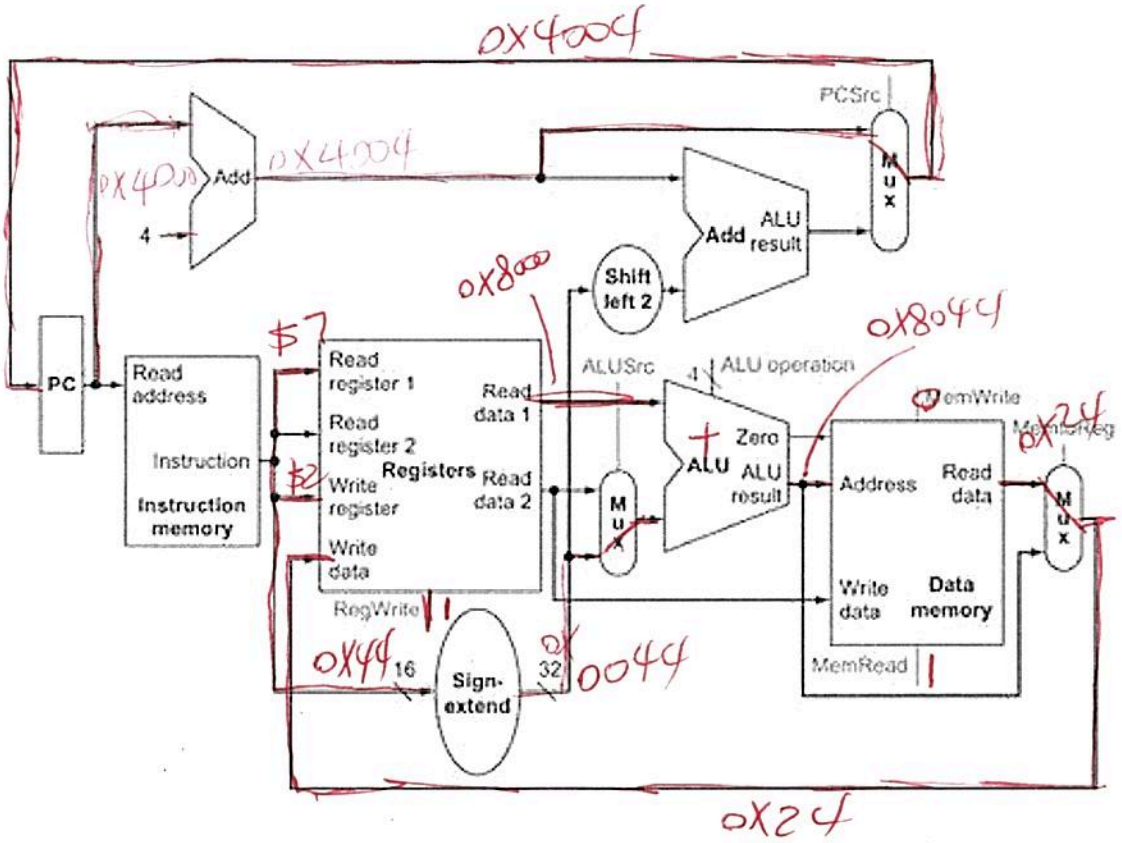
First NAME: KEY Last Name: _____

Problem 1

Highlight the active data path for:

- *lw $2, 0X44($7)*

Annotate the different segments of highlighted datapath with what they carry Assume the instruction is at memory location 0X4000, ($2) = 0X19 , and ($7) = 0X8000, and Mem[0x8000] = 0x40 and Mem[0x8044] = 0x24



After execution:

$2 = 0X24 $7=0X8000 Mem[0x8000]= 0X40 Mem[0x8044] = 0X24 PC= 0X4004

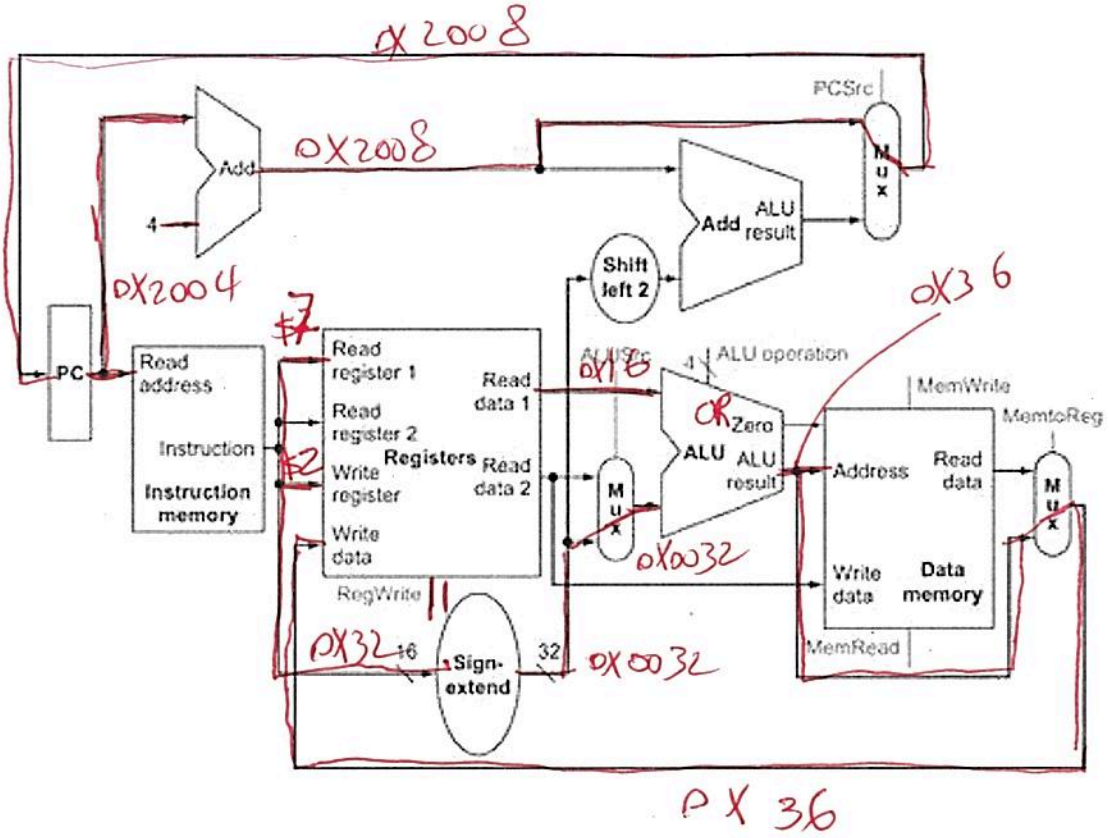
Problem 2

Highlight the active data path for:

- *ori $2, $7, 0x32*

0011 0010
0000 0110
0011 0110 → 0X36

Annotate the different segments of highlighted datapath with what they carry Assume the instruction is at memory location 0X2004, ($2) = 0X9 , and ($7) = 0X16



After execution:

$2 = 0X36 $7= 0X16 PC= 0X2008

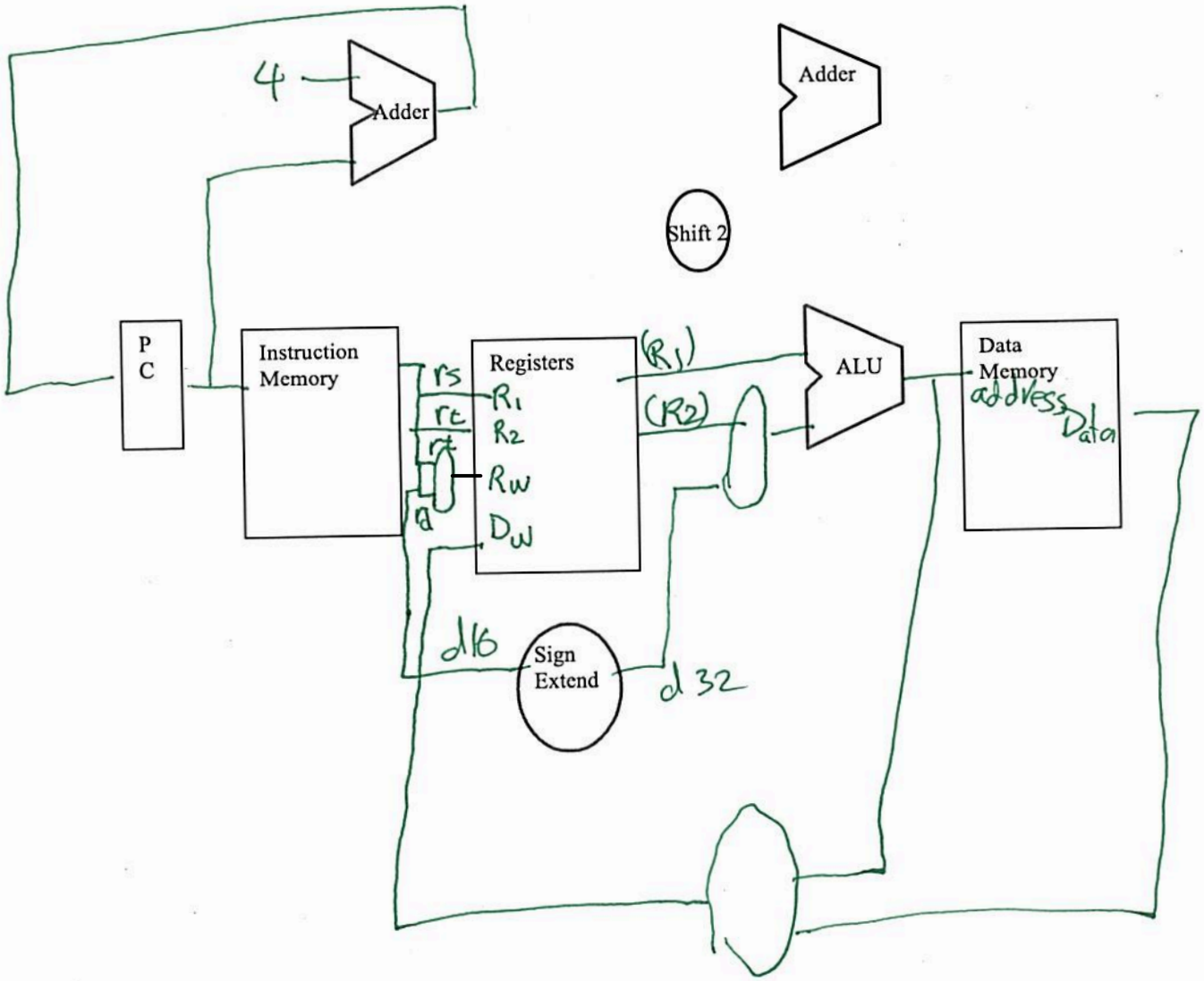
EGC442 Quiz #12 Dr. Izadi

First NAME: Key Last Name: _____

Show the data path for the following instruction set:

- *lw rt, d16(rs),*
- *R-type,*

Make sure only use the components that are essential and cross out the components that are not used. You may need additional components such as multiplexers.



EGC442 Quiz #11 *Dr. Izadi*

First NAME:_____Key_____ Last Name:_____

1. Determine the g_i and p_i values of the following two 4 bit numbers. What is c_4?

0 1 0 1

\+ 1 0 1 1

$g_i = a_i\, b_i$
$p_i = a_i + b_i$
$g_0 = 1$ $p_0 = 1$
$g_1 = 0$ $p_1 = 1$
$g_2 = 0$ $p_2 = 1$
$g_3 = 0$ $p_3 = 1$

$c_4 = g_3 + p_3g_2 + p_3p_2\, g_1 + p_3\, p_2\, p_1\, g_0 + p_3\, p_2\, p_1p_0\, c_0$

$c_4 = 0 + 0 + 0 + 1 + c_0$
$= 1$

2. One simple way to model time for logic is to assume each AND and OR gate takes the same time for a signal to pass through it. Time is estimated by simply counting the number of gates along the longest path through a piece of logic. Compare the number of gate delays for the critical paths of the following 16-bit adders
   a. Ripple carry

      $16 \times 2 = 32$

   b. two-level carry lookahead

$p_i = 1$ $g_i = 1$ gate
$G_0 = {}_{g3} + p_3g_2 + p_3p_2\, g_1 + p_3\, p_2\, p_1\, g_0 = 2$ gate delay
~~$P_0 = p_3\, p_2\, p_1p_0 = 1$ gate dely~~
C4 = G3 + P3G2 + P3P2 G1 + P3 P2 P1 G0 + P3 P2 P1P0 $c_0 = 2$
Total delay = 5

   c. Carry lookahead at level one, and ripple carry between 4-bit modules

$p_i = 1$ $g_i = 1$ gate

$c_4 = g_3 + p_3g_2 + p_3p_2\, g_1 + p_3\, p_2\, p_1\, g_0 + p_3\, p_2\, p_1p_0\, c_0 = 2$ gate delay
Total level 1 = 3 gate delay
Ripple 4 times = $4 \times 3 = 12$

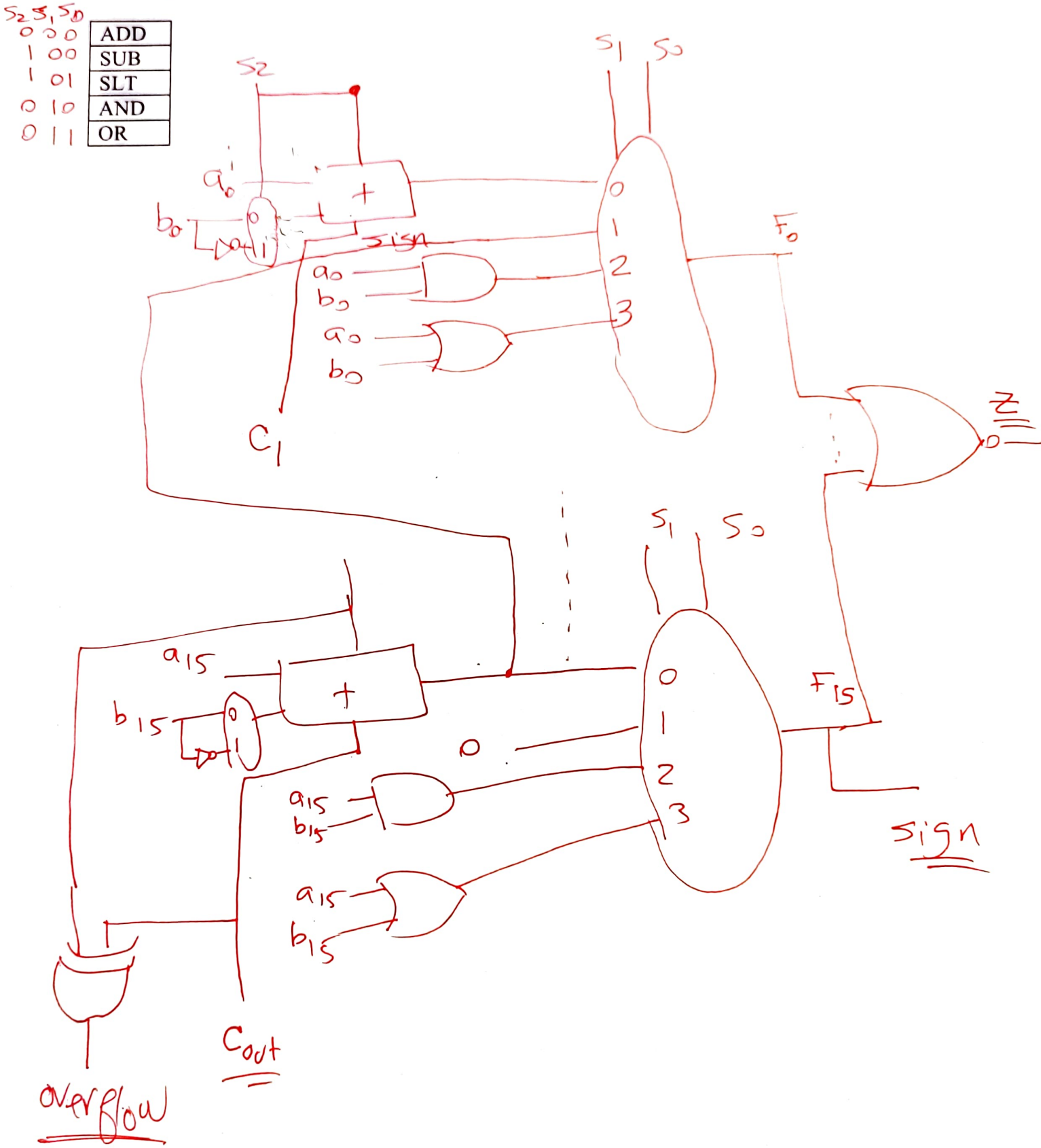
Dr. Izadi

EGC442 Quiz #10

First NAME: key Last Name: _____

1. Design the least significant and most significant modules of a 16 bit ALU with the following functionality. Show the carry, zero, overflow and sign flags for the ALU.

$S_2 S_1 S_0$	
0 0 0	ADD
1 0 0	SUB
1 0 1	SLT
0 1 0	AND
0 1 1	OR



EGC442 Quiz #9 *Dr. Izadi*

First NAME: Key Last Name: _____

25 Points

1) For the third multiplication algorithm, as depicted the following diagram

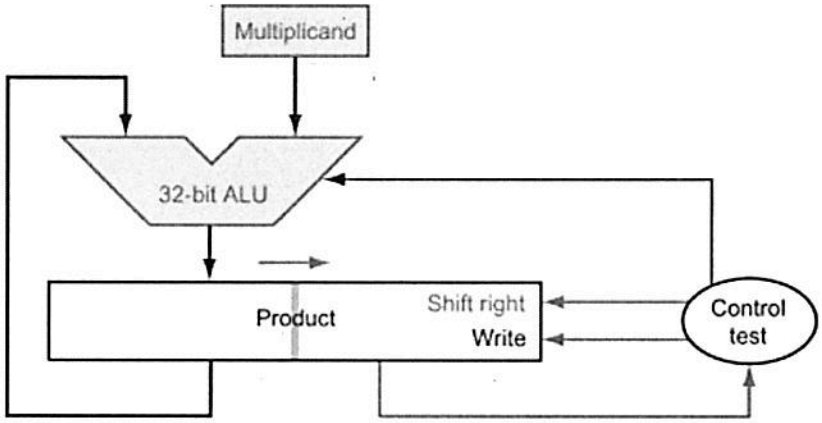


Figure 1: A multiplier

Assuming the following data:

1001 → Multiplicand
× 1101 → Multiplier
→ Products

9
x 13
117

Show step by step how the algorithm performs the multiplicatiton. At each step show the intermediate Multipier, Multiplicand, and Product.

Product

① 0000 1101 ↑ add
1001

1001 1101

② 0100 1110 ← no add

③ 0010 0111 ← add
1001

1011 0111

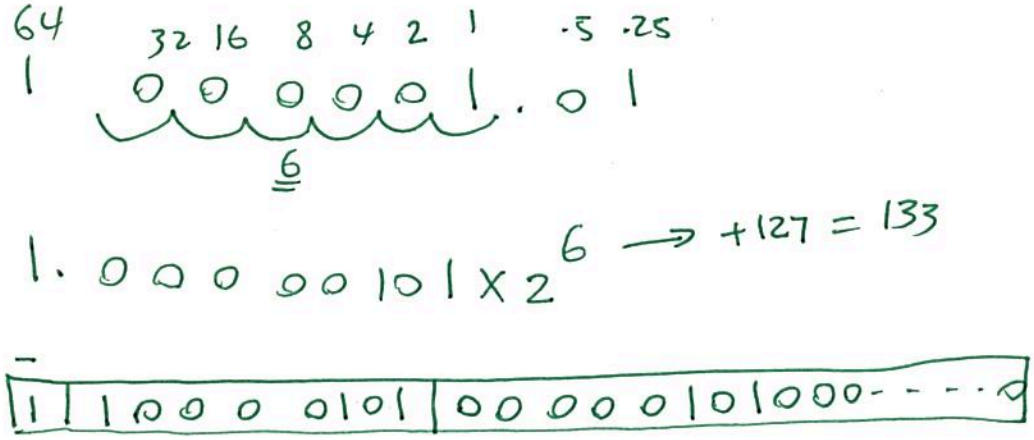
④ 0101 1011 ← add
1001

1110 1011

128 64 32 16 8 4 2 1
0 1 1 1 0 1 0 1 → 117

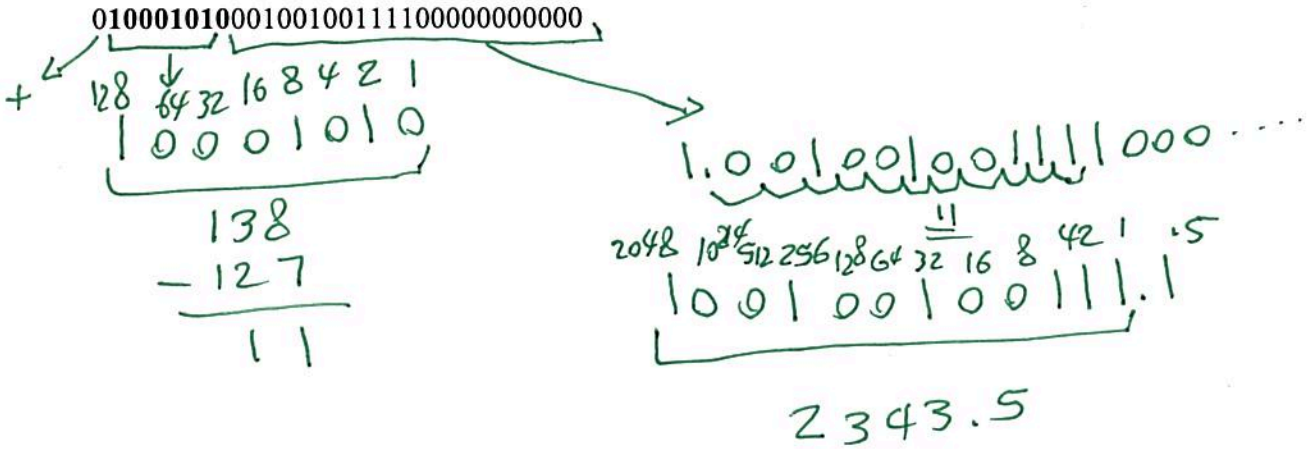
10 Points

2. Show the IEEE 754 binary representation of the number -65.25_{ten} in single precision:



15 Points

3. Convert the single precision binary floating-point representation to decimal.



EGC442 Quiz #8 *Dr. Izadi*

First NAME: Key Last Name: _____

20 Points

1) Given 10011100110001111100010111100010, is it
   a. An assembly code?
   b. A signed 2's complement number?
   c. A unsigned number?
   d. A Machine code?
   e. Could be b., c. or d ?
   f. None of the above

20 Points

2) The largest product resulting from a multiplication of a 16-bit multiplicand and a 16-bit multiplier is 32 bits long.

20 Points

3) Determine the indicated flags for the following data and operation.

```
   1011001
 - 0101101
```

```
  1011001
+ 1010011
---------
 10101100
```

Result = 01011100
CY = 1
Sign = 0
Overflow = 1
Zero = 0

CY=1

40 Points

4) For the first multiplication algorithm, as depicted the following diagram

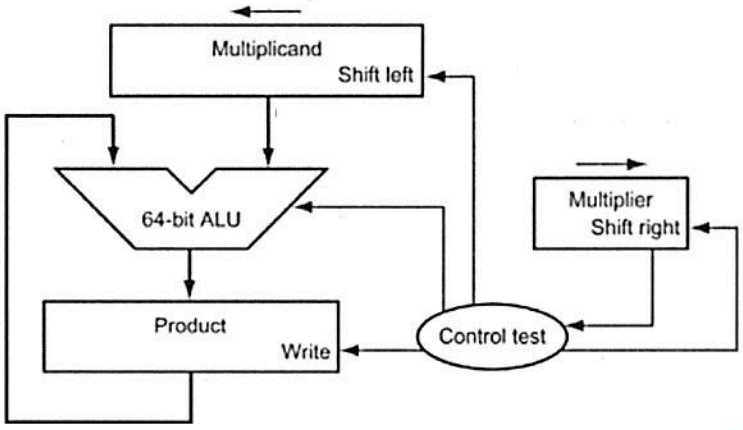


Figure 1: Diagram of a multiplier

1011 11
X 0101 x 5

1 0 1 1
0 0 0 0
1 0 1 1
0 0 0 0
0 0 1 1 1 → 55

Assuming the following data:

1011 → Multiplicand
× 0101 → Multiplier
→ Products

Show step by step how the algorithm performs the multiplicatiton. At each step show the intermediate Multipier, Multiplicand, and Product.

① product 0000 0000
② multiplier 0101 add
product 0000 1011 multiplicat 1011Ø
multiplier 0010 no add
③ product 0000 1011 mutiplicant 101100
multiplier 0001 add

0000 1011
1011 00
product 0011 0111

④ product 0011 0111 multiplicant 1011000
multiplier 0000 no add

product 0011 0111 → 55

EGC442 **Quiz 7** Dr. *Izadi*

First NAME:_____ **Last Name:**_____

15 Pt.

1) A program calls a procedure SWAP two swap variable x and y. Currently, x is in $s1, y is in $s2. How might the program pass the parameter values to Power?

a. add $s2, $a2, $0
   add $s1, $a1, $0
b. add $a2, $s2, $0
   add $a1, $s1, $0
c. add $v2, $s2, $0
   add $v1, $s1, $0
d. None of the above.

35 Pt.

2) Write a leaf procedure SWAP (x, y) to exchange variable x and y. Assume x and y are properly assigned MIPS registers.

```
swap: add $t0, $a1, $0
      add $a1, $a2, $0
      add $a2, $t0, $0
      jr $ra
```

35 Pt.

3) Write a leaf procedure SWAP (x, y, k) to exchange contents of x[k] and y[k]. Assume &x[0] is in $a1, &y[0] is in $a2, and k is in $a3.

```
swap: sll $a3, $a3, 2
      add $a1, $a1, $a3
      add $a2, $a2, $a3
      lw $t0, 0[$a2]
      lw $t1, 0[$a1]
      sw $t1, 0[$a2]
      sw t0, 0[$a1]
      jr $ra
```

15 Pt.

4) A main program calls a SWAP procedure using the instruction: jal swap. That instruction is at address 0x2F000. Upon execution of jal, what happens to $ra?

$ra = 0x2F004

EGC442 Key **Quiz 6** Dr. *Izadi*
First NAME:_____ **Last Name:**_____

45 Pt.

1) Given the following initial values, determine the resulting value for the given operation.
$t1 = 0011 0000 0000 0000 0000 0000 1110 1001
$a2 = 0000 0000 0000 0000 0000 0000 1101 1011
$s1 = 1100 1010 1100 0011 1111 0101 1100 1010

and 0000 0000 0000 0000 0000 0000 1100 1010
OR 1100 1010 1100 0011 1111 0101 1101 1011

a. For the following instruction:
and $t1, $s1, $a2

Only put down the **value of the register that changes in hex**

$s1: _____ $a2:_____ $t1: 0X 0 0 00 00 CA

b. For the following instruction:
or $t1, $s1, $a2

Only put down the **value of the register that changes in hex**

$s1: _____ $a2:_____ $t1: 0X C AC 3 F 5 D B

c. For the following instruction:
nori $t1, $s1, 0x0000

Only put down the **value of the register that changes in hex**

$s1: _____ $a2:_____ $t1: 0X 3 5 3 C 0 A 3 5

0011 0101 0011 1100 0000 1010 0011 0101

Assume $s1 has 0x34 and $s2 has 0x2E. Given this code:

0x49 0x49

```
        bne   $s3, $s4, Else
        add   $s0, $s1, $s2
        j     Exit
Else:   sub   $s0, $s1, $s2
Exit:
```

10 Pt.

2) If $s3 is 0x49 and $s4 is 0x49, which instruction executes after bne?

add $s0, $s1, $s2

10 Pt.

3) If the first instruction were beq rather than bne, what instruction should then appear immediately after beq?

sub $s0, $s1, $s2

35 Pt.

4) Write a sequence of MIPS instruction to perform the following C code

$s1 $s2 $t2 $a1 $a2 $s1

if (i != j)
f = g + h – i;

where i, j, f, g, h are assigned to $s1, $s2, $t2, $a1, $a2 registers, respectively.

```
beq  $s1, $s2, EXIT
add  $t2, $a1, $a2
sub  $t2, $t2, $s1
EXIT:
```

EGC442 **Quiz 5** Dr. *Izadi*

First NAME:_____ **Last Name:**_____

1- 5, each 5 points, 6, 25 points

Assume $s3 has 5004, and words addressed 5000..5002 have the data shown:

5000: 0x99
5001: 0x77
5002: 0x23
5003:0x23
5004:0x6E
5005:0x34
5006:0x13
5007:0x34

1) What address will be computed by:
lw $t0, -4($s3) 5004-4=5000

$t0=0x99772323

2) What value will be put in $t1 by:
lw $t1, -2($s3) 5004 − 2 = 5002

$t1 = 0x23 23 6E34

3) What value will be put in $t2 by:
lw $t2, 0($s3) 5004 + 0 = 5004

$t2 = 0x 6E 34 13 34

4) An array A has a base address of 2000. What is the address of A[2]?

2000 + 4*2 = 2008

5) Assuming $s3 has 5000, is the following an acceptable instruction?
lw $t0, 3($s3)
NO. 5003 is not multiple of 4

6) Assume the base address of array A is in register $s2. Write a sequence of instructions to perform the following operations:
A[2] ← A[0] + A[1]

```
lw  $t0, 0($s2)
lw  $t1, 4($s2)
add $t1, $t1, $t0
sw  $t1, 8($s2)
```

EGC442 **Quiz #4** Dr. *Izadi*

First NAME:_____ **Last Name:**_____

You must show your complete work for full credit!

. 1. Consider the following performance measurements for a program:

	Computer A	Computer B
Number of Instructions	4×10^8	3×10^8
Clock rate	4 GHZ → .25ns	2 GHz → .5ns
CPI	2	1

a. Which computer is faster for that program?

$t_A = 4 \times 10^8 \times 2 \times .25 \times 10^{-9} = 2 \times 10^8 \times 10^{-9} = .2$ sec

$t_B = 3 \times 10^8 \times 1 \times .5 \times 10^{-9} = .15$ sec

B is faster

b. Which computer has a higher MIPS

$MIPS_A = \frac{4 \times 10^8}{10^6 \times .2} = 2000$

$MIPS_B = \frac{3 \times 10^8}{10^6 \times .15} = 2000$

same

2. A program runs in 120 seconds. Multiply and divide operations are responsible for 40 and 60 of those seconds, respectively. Would it be possible to run the program 2 times faster

a. By improving the multiplication alone. If yes, by what factor? NO
b. By improving the division alone. If yes, by what factor? NO
c. By improving the multiplication and division by the same factor. If yes, by what factor? 2.5 times

M D other

$120 = 40 + 60 + 20$

a. $60 \neq 0 + 80$

b. $60 \neq 0 + 60$

c. $60 = 40 + 20$

$\frac{100}{40} = 2.5$ times

3. Given: b = 2, c = 5, d = 1,
   add t, d, c → 5 + 1 → 6
   sub a, t, b → 6 − 2 = 4
   Final value of a 4 and b 2

4. Order the assembly instructions to calculate the expression: a = b + c - d + e

- add t0, b, c (1)
- sub a, t0, d (3)
- add t0, t0, e (2)

EGC442 **Quiz #3** Dr. *Izadi*

First NAME: Key **Last Name:**_____

1. Computer A's performance is 4 times as fast as the performance of computer B, which runs a given application in 20 seconds. How long will computer A take to run that application?

$$t_A = \frac{t_B}{4}$$

$$t_A = \frac{20}{4} = 5 \text{ sec}$$

2. Our favorite program runs in 40 seconds on computer A, which has a 2 GHz clock. We are trying to help a computer designer build a computer B, which will run this program in 14 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.4 times as many clock cycles as computer A for this program. What is the CPU clock cycles for computer B?

$t_A = 40$ $f_A = 2\times10^9$ N_A

$t_B = 14$ $f_B = ?$ $1.4N_A$

$$t_A = 40 = \frac{N_A \times CPI \times .5\,ns}{14 = 1.4N_A \times CPI \times T_B} = T_B = \frac{14\times.5}{40\times1.4} = \frac{1}{8}\,ns = 0.125\,ns$$

$f_B = 8$ GHz

3. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 125 ps and a CPI of 4.0 a program with 2 X 10^6 instructions, and computer B has a clock cycle time of 250 ps and a CPI of 2.4 for the same program.

   a. Which computer executes fewer clock cycles? B
   b. Which computer has the smaller execution time? A

$T_A = 125$ ps $CPI_A = 4$ $N = 2\times10^6$

$T_B = 250$ ps $CPI_B = 2.4$ $N = 2\times10^6$

$CLK_A = 4\times2\times10^6 = 8\times10^6$

$CLK_B = 2.4\times2\times10^6 = 4.8\times10^6$

b.

$CPU_{TA} = 8\times10^6 \times 125\times10^{-12} = 1$ ms

$CPU_{TB} = 4.8\times10^6 \times 250\times10^{-12} = 1.2$ ms

4. A compiler designer is trying to decide between two code sequences for a particular computer. The hardware designers have supplied the following facts:

	CPI for each instruction class		
	A	B	C
CPI	1	2	3

For a particular high-level language statement, the compiler writer is considering two code sequences that require the following instruction counts:

Code sequence	Instruction counts for each instruction class		
	A	B	C
1	1	3	2
2	4	2	1

6
7

a. Which code sequence executes the largest number of instructions?

Code 2

7

b. Which code sequence executes the largest number of clock cycles?

Code 1 = 1X1 + 2X3 + 3X2 = 13

Code 2 = 1X4 + 2X2 + 3X1 = 11

Code 1

EGC442 **Quiz #2** Dr. *Izadi*

First NAME: Key **Last Name:** _____

1. Match the situation with the closest analog of a great idea in computer architecture.

d
b
a
c

- **Make the Common Case Fast**
- **Hierarchy of Memories**
- **Design for Moore's Law**
- **Use Abstraction to Simplify Design**

   a. A soccer player runs not to where the ball is, but to where the ball will be.

   b. A customer talks to a phone agent. If there's a problem, he talks to the agent's supervisor.

   c. A house architect first designs a house with 5 rooms, then designs room details like closets, windows, and flooring.

   d. A college student rents an apartment closer to campus than to her favorite weekend beach spot.

2. The following could be a machine-language instruction: 1000110010100000.

   ☒ True

   ☐ False

3. The following could be an assembly language instruction: 1000110010100000.

   ☐ True

   ☒ False

4. An assembler translates assembly language instructions like *add A,B* to machine-language instructions like 1000110010100000.

   ☒ True

   ☐ False

5. Which is a high-level language instruction?

   ☐ 00000000101000100000000100011000

   ☐ add $2, $4, $2

   ☒ temp = v[k];

6. What kind of language is C?
   - ☐ Machine
   - ☐ Assembly
   - ☒ High-level

7. The five components of a computer.

d
- **Control**

a
- **Input**

c
- **Memory**

b
- **Output**

e
- **Datapath**

   a. Writes data to memory. Ex: Keyboard.

   b. Reads data from memory. Ex: Display.

   c. Stores instructions and data.

   d. Sends signals that determine the operation of the other components.

   e. Performs computations.

8. An integrated circuit is often called a _____.
   - ☒ chip
   - ☐ CPU

9. The CPU chip physically occupies _____ of the size of the iPad 2.
   - ☐ most
   - ☒ a small fraction

10. A CPU is also known as _____.
   - ☐ a datapath
   - ☐ control
   - ☒ a processor

EGC442 **Quiz #1** *Dr. Izadi*

First NAME: Key **Last Name:** _____

1. Convert $(A4.C)_{16}$ directly to base 2 and base 8.

Base 2

1010 0100.1100

2 4 4.6

244.6

2. Using a total of 8 bits, represent -65 in signed 2's complement format.

1011 1111

S 64 32 16 8 4 2 1

\- 0 1 0 0 0 0 0 1

3. The given numbers are represented in signed 2's complement. Carry out the indicated operation and specify the indicated flags.

11001010
\- 01111011

1 1 0 0 1 0 1 0
1 0 0 0 0 1 0 1

0 1 0 0 1 1 1 1

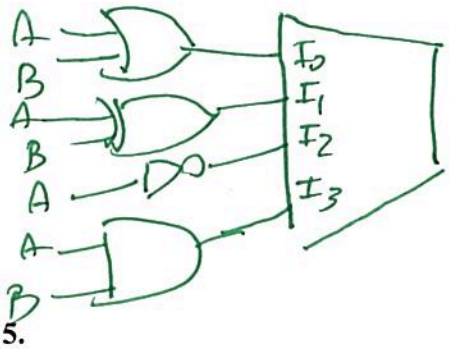
0100 1111

GCY=1

\- \- —— +

Carry = 1 Sign = 0 Overflow = 1

4. Using gates and multiplexer(s), design a one-bit ALU that performs the following logical operations:



S_1	S_0	Function
0	0	OR
0	1	XOR
1	0	NOT
1	1	AND

5.

a. Utilizing the block diagram of 4- bit registers, multiplexers, decoders, and any other needed gates, design a register file with 4 4-bit registers such that it can allow reading of any two registers and writing of any one.

b. Indicated how many bits each line in the following block diagram represent.