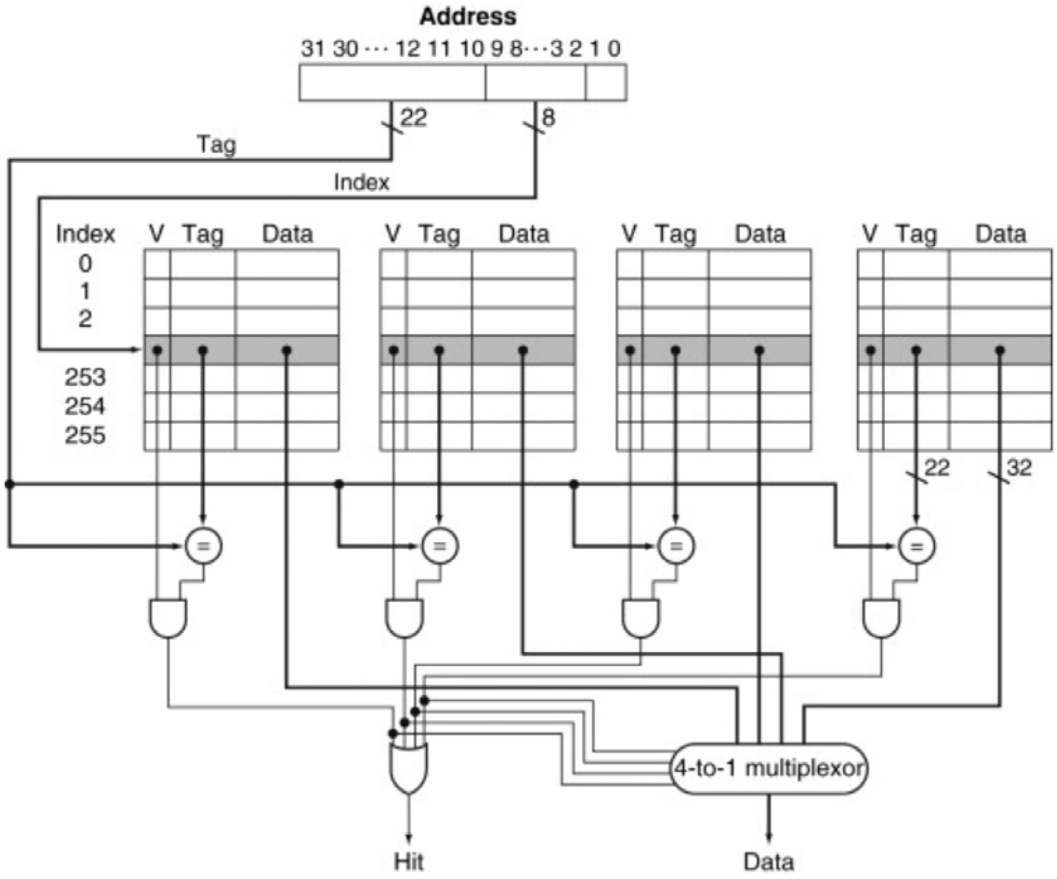
First Name:_____Last Name: _____

1) Assume a two-way set-associative cache with one byte word size, 4-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 7, 6. Show the hits and misses and final cache contents.

2) Assume a fully associative cache with 4-one word blocks. Given the following sequence of block addresses, indicate if each request results in a cache hit or miss: 1, 9, 6, 5, 7, 6. Show the hits and misses and final cache contents.

3) What kind of cache memory is depicted below:



4) The_____of every cache block within the appropriate set of a set-associative cache is checked for a match against the memory block address.

- index
- tag
- block offset

5) A four-way set-associative cache with 32-one word blocks requires_____comparators to compare the tags of each element within the set.

- 4
- 8
- 32

6) A direct mapped cache with 32-one word blocks requires_____comparator(s) to compare the tags of of an element with the memory block address.

- 1
- 32

7) Which block in the cache is replaced by memory block 29?

Cache configuration: 4-way set-associative cache with 8-one word blocks
Replacement scheme: LRU
Sequence of previously accessed block addresses: 5, 13, 21, 13, 5

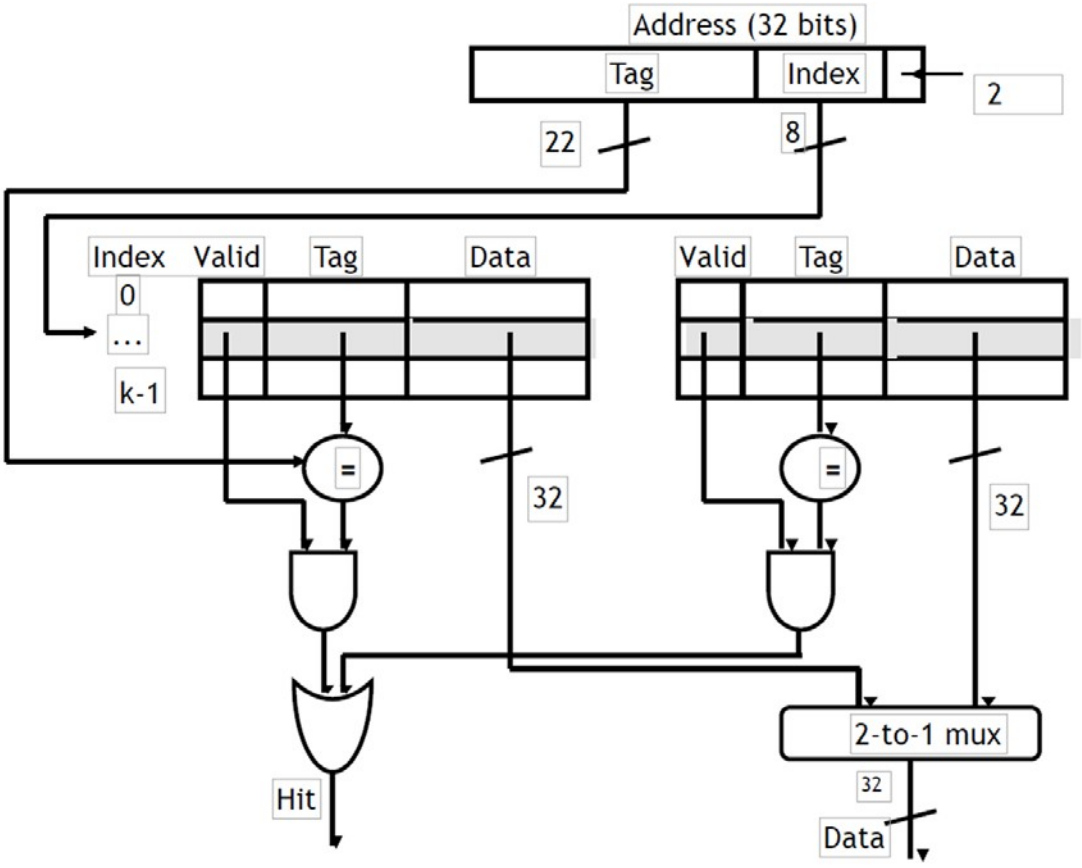
- Mem[5]
- Mem[13]
- Mem[21]
- None. An element in set 1 is unused, so Mem[29] is placed in the fourth element of set 1.

8) Design a two ways set associative cache with the following parameters:

- Address size: 32 bits
- Cache data size: 4 KB
- Cache block: 1 word (4 bytes)

9) For the following depicted diagram

a. Identify the cache architecture
b. What is the total cache size in words?
c. What is the index and tag when accessing memory location 0x0034FC08?



10) The following is a series of address references given as word addresses: 9, 4, 20, 4, 8, 15, 5, 19, 4, 20, 4, 22, 7, 17, 10. Assume a cache with a capacity of 16 words and the word size of 1 byte

a. For two ways set associative, show the hits and misses and final cache contents.

Location	Hit/Miss?
9	
4	
20	
4	
8	
15	
5	
19	
4	
20	
4	
22	
7	

b. For a fully associated cache, show the hits and misses and the final cache contents.

11) Assume an instruction cache miss rate for an application is 2% and the data cache miss rate of 4%. Assume further that our CPU is running at 2 GHz and has a CPI of 2 without any memory stalls. The main memory access time is 100 ns.
a. Determine the overall CPI with the indicated misses, provided the frequency of all loads and stores in the application is 20%.
b. Suppose we like to add a second level cache with an access time of 5 ns, which has an instruction miss rate of .5% and data cache miss rate of .8%. Determine the overall CPI.