First Name:_____ Last Name: _____

1) Assume a direct-mapped cache with 32 blocks and a block size of 8 bytes.

a) Byte address 400 maps to block address _____.
b) Byte address 400 maps to block number _____.
c) Byte address 360 maps to block number _____.

2) The miss rate may increase if the block size becomes a significant fraction of the cache size.

- True
- False

4) The processing of a cache miss creates a _____.

- pipeline stall
- interrupt

5) If an instruction access results in a miss, then the address of the instruction at _____ is fetched from the memory.

- PC
- PC - 4
- PC + 4

6)

Write Through	Write Back Scheme	Write Buffer
A value is read from the cache and modified. The modified value is written to the cache and the corresponding memory location.		
A value is read from the cache and modified. The modified value is written to the cache and to a queue that stores the value while waiting to be written to the corresponding memory location.		
A value is read from the cache and modified. The modified value is written to the cache. The modified value is only written from the cache to memory when the cache block is replaced.		

7) Assume the miss rate of an instruction cache is 3% and the miss rate of the data cache is 6%. If a processor has a CPI of 2 without any memory stalls, and the miss penalty is 200 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 25%.

a. The instruction cache miss rate is _____.
b. he number of memory-stall cycles for data misses in terms of the instruction count (I) is _____.
c. The total CPI is _____.

8) Find the AMAT for a processor with a 2 ns clock cycle time, a miss penalty of 40 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls.

9) If the clock rate is increased without changing the memory system, the fraction of execution time due to cache misses _____ relative to total execution time.

- increases
- decreases

10) AMAT considers the average time to access data for _____.

- misses
- both hits and misses

11) Design a direct-mapped cache with the following parameters:

- Address size: 32 bits
- Cache data size: 2 KB
- Cache block: 2 word

12) The following is a series of address references given as word addresses: 9, 4, 20, 4, 8, 15, 5, 19, 4, 20, 4, 22, 7, 17, 10. Assume direct map with **a word size of 1 byte, a block size of 2 words and a total size of 16** words. Show the hits and misses and final cache contents. Show the final cache content.

Location	Hit/Miss?
9	
4	
20	
4	
8	
15	
5	
19	
4	
20	
4	
22	
7	

13) Assume an instruction cache miss rate for an application is 2% and the data cache miss rate of 4%. Assume further that our CPU has a CPI of 2 without any memory stalls and the miss penalty is 40 cycles for all misses.
a. Determine the overall CPI with the indicated misses, provided the frequency of all loads and stores in the application is 20%.

b. Suppose we increase the performance of the machine in the above example by reducing its CPI from 2 to 1 via pipelining. Determine the new overall CPI.