

First Name: _____ Last Name: _____

- 1) Bob is building a fence behind his house. He uses a hammer to attach a board to the rail. Bob then measures and cuts the next board.

The likelihood that Bob will need the hammer again is an example of _____ locality.

- spatial
 temporal

- 2) Bob is building a fence behind his house. He grabs a hammer from the garage. Bob will likely need additional tools stored in the garage, so Bob also grabs nails, a shovel, and a level.

The likelihood that Bob will need resources stored together in the garage is an example of _____ locality.

- spatial
 temporal

- 3) Given the following loop, the high likelihood of accessing multiple elements within array A is an example of _____ locality.

```
while (i < 10){  
    A[i] = A[i] + 2;  
    i = i + 1;  
}
```

- spatial
 temporal

- 4) Given the following loop, the high likelihood of accessing $i = i + 1$ repeatedly is an example of _____ locality.

```
while (i < 10){  
    A[i] = A[i] + 2;  
    i = i + 1;  
}
```

- spatial
 temporal

- 5) Instructions may exhibit temporal locality, but not spatial locality.

- True
 False

6) Data may exhibit spatial locality, but not temporal locality.

- True
- False

7) A memory hierarchy is composed of an upper level and a lower level. Data is requested by the processor. 9 out of 10 requests find the data in the upper level and returns the data in 0.4 ns. The remaining requests require 0.7 ns to return the data.

Determine the corresponding values for the upper level memory.

- 0.4
- 0.9
- 0.1
- 0.7

Hit rate

Miss rate

Hit time

Miss penalty

Select the memory technology that most closely matches the statements below.

8)Used to implement the memory levels closest to the processor.

- SRAM
- DRAM

9)Has fewer transistors per bit of memory.

- SRAM
- DRAM

10)Requires a periodic refresh.

- SRAM
- DRAM

11)Magnetic disk access times.

- Rotational latency
- Transfer time
- Seek time

The time required to move the head to the desired track.

The time required for the desired sector to rotate under the head.

The time required to transfer a block of bits.

A magnetic disk is a type of _____.

- mechanical device
- semiconductor memory

12)Writes to the same location in a _____ can wear out memory bits.

- flash memory
- magnetic disk

13)Memories in personal mobile devices are typically _____.

- flash memory
- magnetic disk

14)In a magnetic disk, sequential block numbers are placed next to one another on a track. Ex: Block 207 is placed after block 206.

- True
- False

15)Magnetic disks are volatile.

- True
- False

Determine the cache index given the direct-mapped cache size and block address. Type the cache index as a binary value. Ex: 110

16)Direct-mapped cache size: 8 one-word blocks, Block address: 00011₂

17)Direct-mapped cache size: 8 one-word blocks, Block address: 10101₂

18)Direct-mapped cache size: 8 one-word blocks, Block address: 10000101₂

19)Direct-mapped cache size: 16 one-word blocks, Block address: 00101100₂

20) A request to address 00101_{two} results in a cache _____.

Index	V	Tag	Data
000	N		
001	Y	00_{two}	Memory (00001_{two})
010	N		
011	Y	11_{two}	Memory (11011_{two})
100	Y	11_{two}	Memory (11100_{two})
101	N		
110	Y	01_{two}	Memory (01110_{two})
111	Y	10_{two}	Memory (10111_{two})

- hit
 miss

21) After a request to address 00110_{two} , the tag in cache block 110_{two} is ______{two}.

Index	V	Tag	Data
000	N		
001	Y	00_{two}	Memory (00001_{two})
010	N		
011	N		
100	Y	11_{two}	Memory (11100_{two})
101	N		
110	N		
111	Y	10_{two}	Memory (10111_{two})

- 10
 00

22) A request to address 00001_{two} results in a cache _____.

Index	V	Tag	Data
000	Y	01_{two}	Memory (01000_{two})
001	Y	11_{two}	Memory (11001_{two})
010	Y	01_{two}	Memory (01010_{two})
011	Y	00_{two}	Memory (00011_{two})
100	N		
101	N		
110	N		
111	N		

- hit
 miss

23) After a request to address 00101_{two} , the data in cache block 101_{two} is Memory(_____ $_{two}$).

Index	V	Tag	Data
000	Y	01_{two}	Memory (01000_{two})
001	N		
010	N		
011	Y	00_{two}	Memory (00011_{two})
100	N		
101	Y	11_{two}	Memory (11101_{two})
110	Y	00_{two}	Memory (00110_{two})
111	N		

- 11101
- 00101

24) A request to address 10111_{two} results in a cache _____.

Index	V	Tag	Data
000	N		
001	N		
010	Y	11_{two}	Memory (11010_{two})
011	N		
100	Y	10_{two}	Memory (10100_{two})
101	N		
110	Y	00_{two}	Memory (00110_{two})
111	Y	10_{two}	Memory (10111_{two})

- hit
- miss

25) After a request to address 10000_{two} , the data in cache block 000_{two} _____.

Index	V	Tag	Data
000	Y	10_{two}	Memory (10000_{two})
001	Y	00_{two}	Memory (00001_{two})
010	Y	11_{two}	Memory (11010_{two})
011	Y	11_{two}	Memory (11011_{two})
100	Y	10_{two}	Memory (10100_{two})
101	Y	00_{two}	Memory (00101_{two})
110	Y	00_{two}	Memory (00110_{two})
111	Y	10_{two}	Memory (10111_{two})

- is empty
- does not change

26) Cache block 111_{two} with tag 00_{two} corresponds to memory address ______{two}.

- 11100
- 00111

27) Design a direct-mapped cache with the following parameters:

- Address size: 32 bits
- Cache data size: 2 KB
- Cache block: 1 word

28) The following is a series of address references given as word addresses: 9, 4, 20, 4, 8, 15, 5, 19, 4, 20, 4, 22, 7, 17, 10. Assume direct map with a word size of 1 and a total size of 8 words. Show the hits and misses and final cache contents. Show the final cache content.

Location	Hit/Miss?
9	
4	
20	
4	
8	
15	
5	
19	
4	
20	
4	
22	
7	
17	
10	