First Name:_____ Last Name: _____

1) When an exception occurs in MIPS, the processor first saves the address of the offending instruction in the _____.

2) In MIPS, the _____ register stores the cause of an exception and communicates that information to the operating system for exception handling.

3) For a vectored interrupt, the cause of an exception determines the _____ that control is transferred to.

4) In a pipeline implementation, offending arithmetic overflow instructions are detected in the _____ stage of the pipeline to prevent the results from being written to the _____ stage.

- IF, ID
- EX, MEM
- EX, WB

5) Five-stage pipeline (IF, ID, EX, MEM, WB) executes the following instruction sequence:

```
add $1, $2, $1  # arithmetic overflow
XXX $1, $2, $1  # undefined instruction
sub $1, $2, $1  # hardware error
```

Which exception should be recognized first in the above sequence?

- arithmetic overflow
- undefined instruction
- hardware error

6) In the majority of MIPS implementations, multiple thrown exceptions are interrupted _____.

- according to which instruction causes the largest exception
- according to which offending instruction is earliest
- randomly

7) Given this instruction sequence,

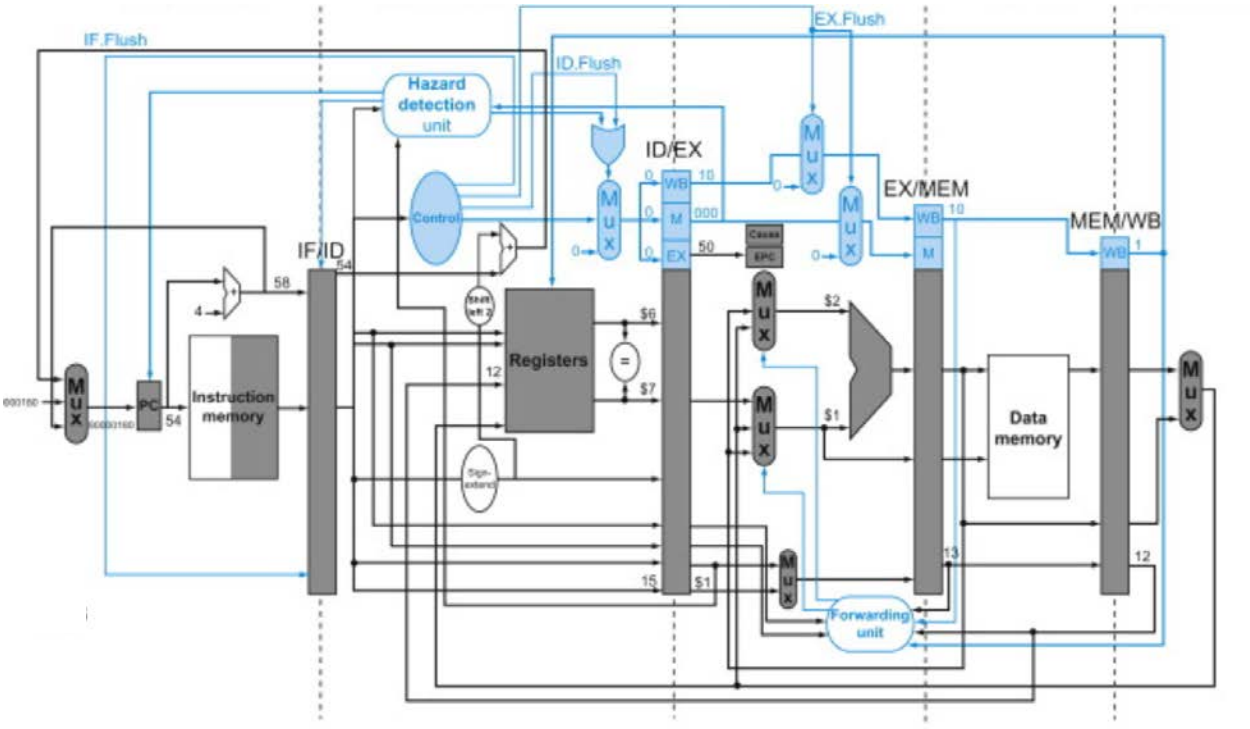
```
40hex   sub  $11, $2, $4
44hex   and  $12, $2, $5
48hex   or   $13, $2, $6
4Chex   add   $1, $2, $1
50hex   slt  $15, $6, $7
54hex   lw   $16, 50($7)
...
```

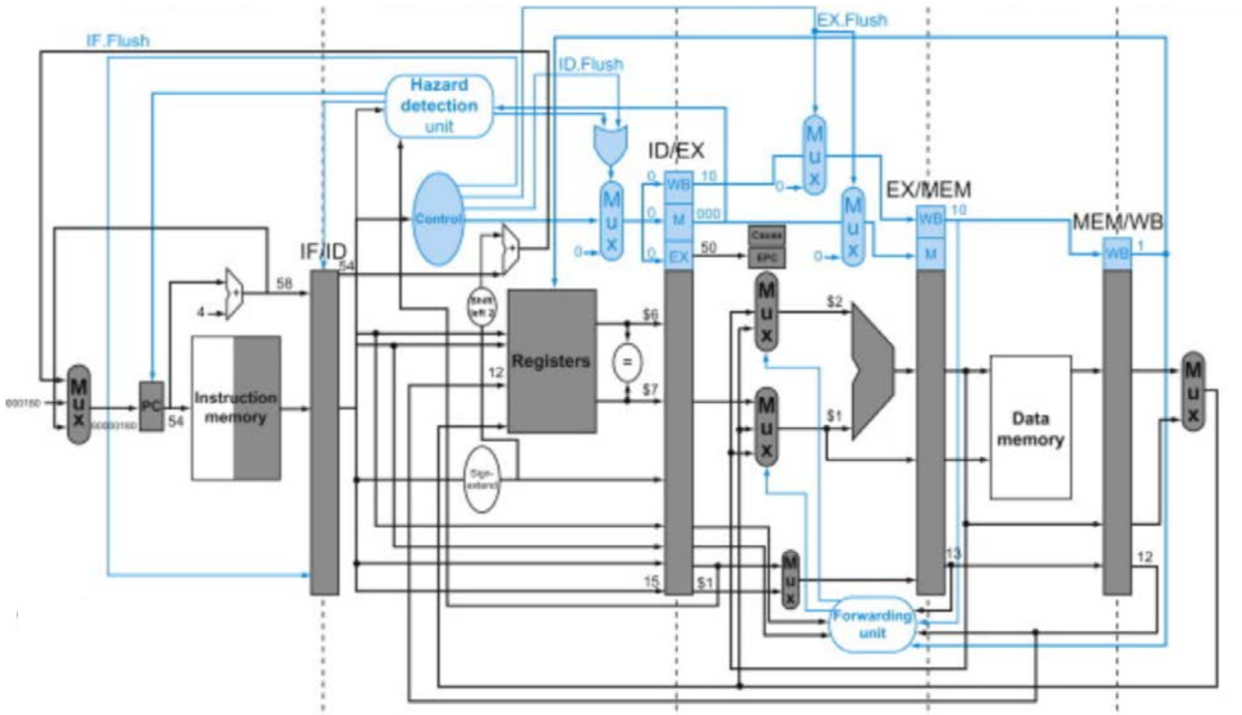
assume the instructions to be invoked on an exception begin like this:

```
80000180hex   sw     $26, 1000($0)
80000184hex   sw     $27, 1004($0)
...
```

Show what happens in the pipeline if an overflow exception occurs in the and instruction.

or $13,$2,$6 **and $12,$2,$5** **sub $1,$2,$4**




IF.Flush
Hazard detection unit
ID.Flush
EX.Flush
ID/EX
EX/MEM
MEM/WB
IF/ID
Control
Registers
Instruction memory
Data memory
Forwarding unit
PC
Mux
WB
M
EX
Cause
EPC
$6
$7
$2
$1
$1
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54
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13
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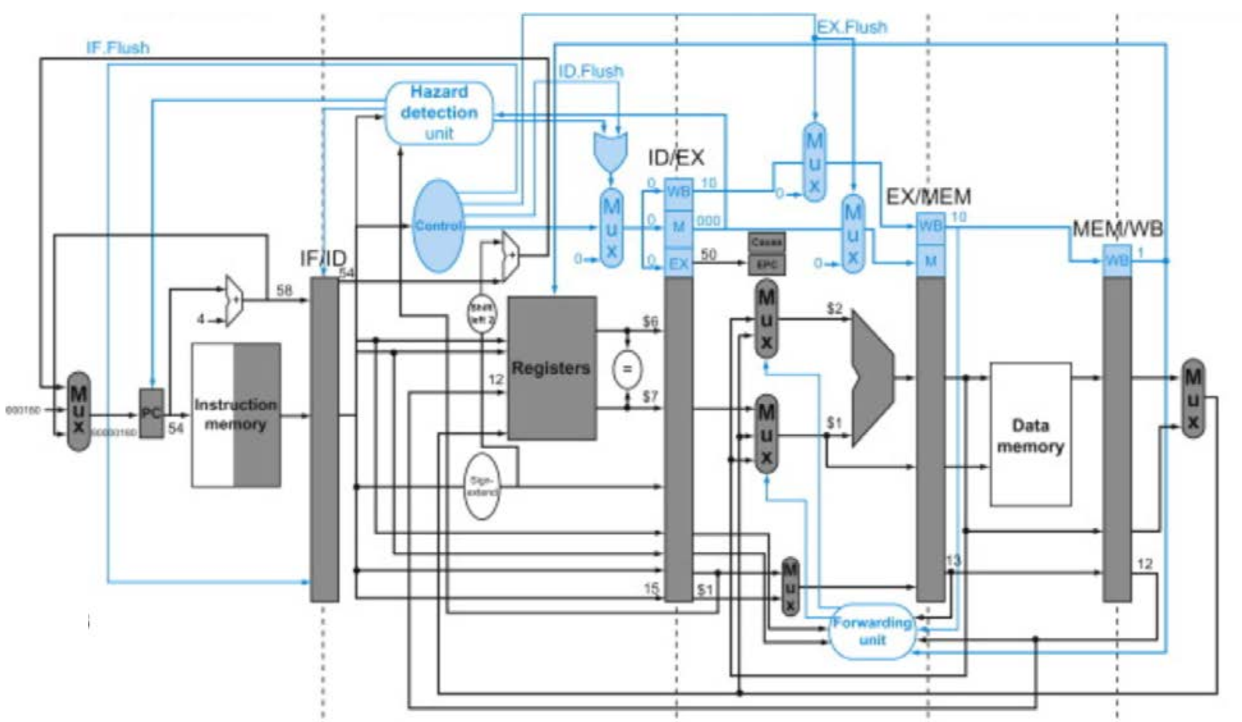
IF.Flush
Hazard detection unit
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$6
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8.

- **single issue**
- **ILP**
- **multiple issue**
- **issue slots**
- **static multiple issue**
- **dynamic multiple issue**

When one instruction is launched per clock cycle.

The parallelism between instructions.

When multiple instructions are launched per clock cycle.

A multiple issue implementation where decisions are made during execution by the processor.

The positions available to issue instructions in a given clock cycle.

A multiple issue implementation where decisions are made by the compiler before execution.

9. Show would the following loop can be scheduled on a static two-issue pipeline for MIPS?

```
Loop:   lw    $t0, 0($s1)
        sub   $t0,    $t0, $a3
        addi  $s1, $s1, -1
        bne   $s1, $0, Loop
```

Reorder the instructions to avoid as many pipeline stalls as possible. Computer the overall IPC.

10) A very long instruction word (VLIW) architecture groups multiple operations together and then launches them like a single instruction.

- True
- False

11) In all static multiple issue processors, the compiler is responsible for removing all data hazards and avoiding all dependences.

- True
- False

12) If the use latency for a load instruction is one clock cycle, then an instruction can use the result from the load on the next clock cycle.

- True
- False

13) Both loop unrolling and register renaming allow a processor to better schedule instructions and improve performance.

- True
- False

14) Loop unrolling and register renaming can lead to an increase in code and the need for more resources.

- True
- False

15) Show would the following loop unrolling and register renaming can be used for 4 iteration of the following on a static two-issue pipeline for MIPS?

```
Loop:   lw    $t0, 0($s1)
        sub   $t0,   $t0, $a3
        addi  $s1, $s1, -1
        bne   $s1, $0, Loop
```

Computer the overall IPC.