EGC442 Problem Set 16 Dr. Izadi

First Name:_____ Last Name: _____

1) In processor X's pipeline, an add instruction in stage 3 should use the ALU. A branch instruction in stage 4 also should use the ALU. Both instructions cannot simultaneously use the ALU. Such a situation is a structural hazard.

- True
- False

2) MIPS implementations tend to have numerous structural hazards.

- True
- False

3) Given the following set of instructions,

a. Identify all the dependencies.
b. Indicate which dependency results in data hazard.
c. Using NOP's, remove all data hazards.
d. How many clock cycles does it take to execute the code segment?
e. Rearrange the code in such a way that the overall result is not altered and the number NOP's used is minimized.
f. How many clock cycle would code in part e takes?

```
lw   $t1, 0($t0)
lw   $t2, 4($t0)
add  $t3, $t1, $t2
sw   $t3, 12($t0)
lw   $t4, 8($t0)
add  $t5, $t1, $t4
sw   $t5, 16($t0)
```

4) Does the following cause a data hazard for the 5-stage MIPS pipeline?

```
add $s0, $s1, $s2
add $s3, $s0, $s4
```

- Yes
- No

5) For the code below,

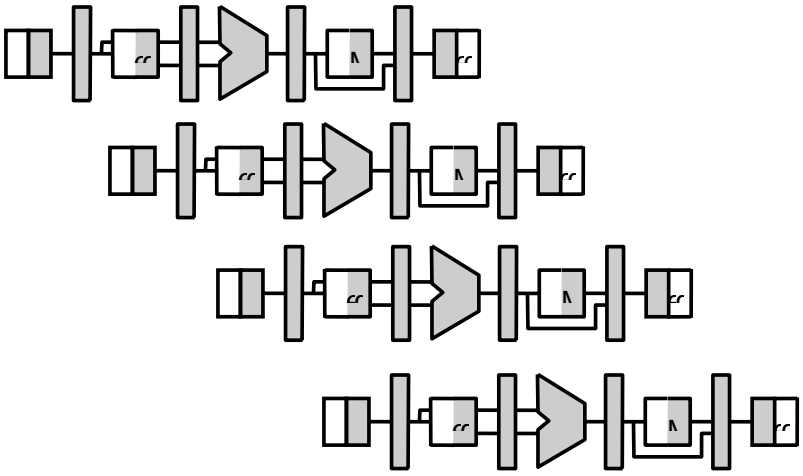
a. On the diagram, mark and identify all the data dependencies in the code given below and identify which dependencies will cause data hazards without forwarding hardware.

sub *$4, $2, $9*

add *$9, $4, $5*

sub *$2, $3, $4*

and *$5, $4, $6*



b. Assuming there is no special hardware that is added for forwarding. Add “nop” instructions to the code to avoid the data hazards.

c. How many clock cycles does it take to execute the code in part b.

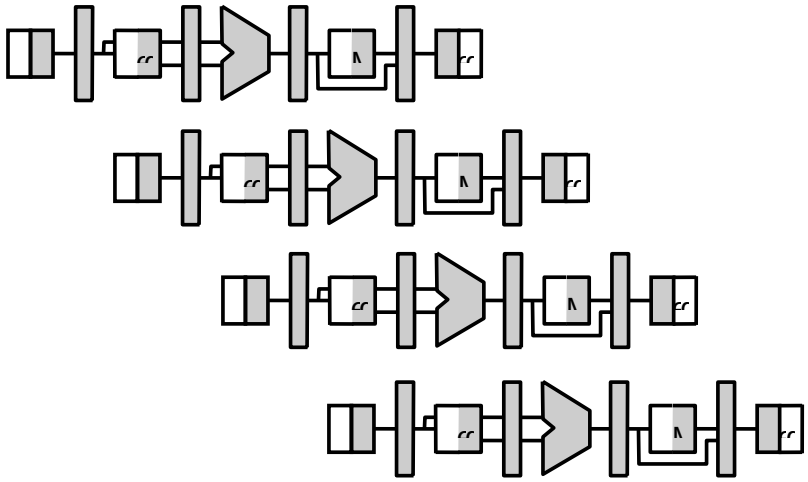
d. Using forwarding, clearly show how it can be use to resolve data hazrds

sub *$4, $2, $9*

add *$9, $4, $5*

sub *$2, $3, $4*

and *$5, $4, $6*



e. How many clock cycles does part d takes.

f. Indicate what each stage will do during the 5^{th} clock cycle.