EGC442 Problem Set 15 Dr. Izadi

First Name:_____ Last Name: _____

1) How many stages exist in the laundry analogy?

2) If laundry is done sequentially, how many minutes do 60 loads take to wash?

3) If laundry is done in a pipelined manner, execution is nearly 4 times faster than if done sequentially. Suppose doing 50 loads sequentially requires 6000 minutes. How long would those 50 loads take if done in a pipelined manner? Assume a 4 times speedup (ignore the fact that some stages are unused for the first few and last few loads).

4) Each load of laundry takes 4 × 30 = 120 minutes to wash, dry, fold, and store (30 minutes each). How many minutes are required to complete one load of laundry when multiple loads of laundry are done in a pipelined manner?

Refer to nonpipelined and pipelined MIPS instruction execution.

5) The nonpipelined datapath implementation has how many stages?

- 1
- 5

6) The pipelined datapath implementation has how many stages?

- 1
- 5

7) The above figure shows the five stages as: Instruction fetch, Reg, ALU, Data access, and Reg. Are the two Regs doing the same thing?

- Yes
- No

8) Does every instruction require all 5 stages?

- Yes
- No

9) Suppose Instr1 is fetched in stage 1. Instr1 then proceeds to stage 2, Reg read. In a pipelined implementation, can Instruction2 be fetched simultaneously with that Reg read?

- Yes
- No

10) On computer X, a nonpipelined instruction execution would require 12 ns, and thus 12 ns exists between instructions. A pipelined implementation uses 6 equal-length stages of 2 ns each, resulting in _____ ns between instructions.

- 1
- 2

11) On computer X, a nonpipelined instruction execution would require 12 ns. A pipelined implementation uses 6 equal-length stages of 2 ns each. Assuming one million instructions execute and ignoring empty stages at the start/end, what is the speedup of the pipelined vs. non-pipelined implementation?

- 2
- 6

12) Match the pipeline stage with the physical resource whose icon represents that stage in the stylized datapath depictions.

- **IM**
- **Reg (write)**
- **DM**
- **ALU**
- **Reg (read)**

Stage 1: IF (instruction fetch)

Stage 2: ID (instruction decode)

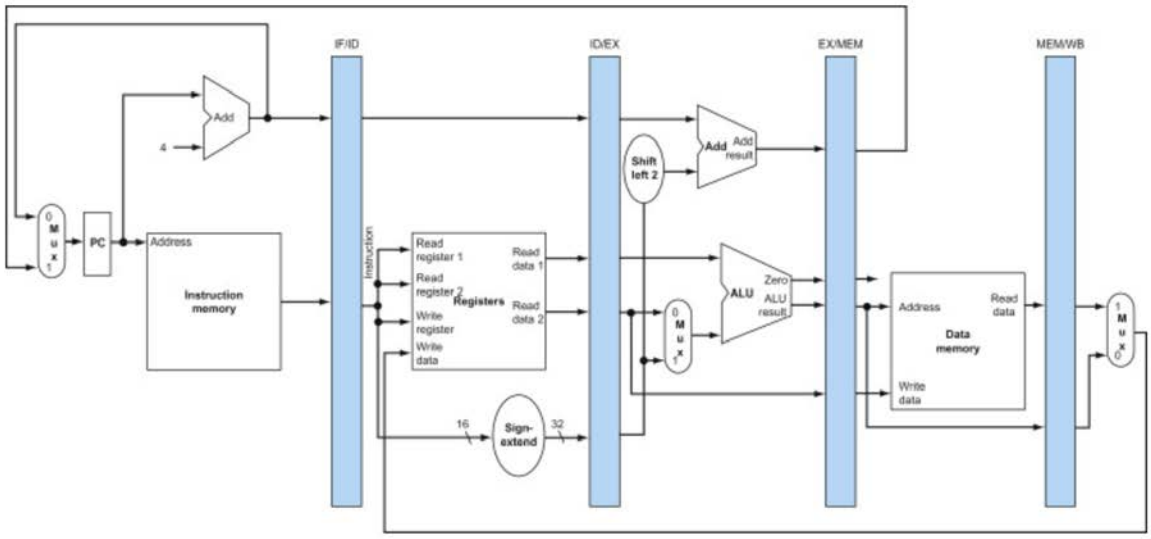
Stage 3: EX (execute)

Stage 4: MEM (data memory access)

Stage 5: WB (write back)

13) Using multiple copies of the following diagram, show the active stages for execution of the following sequence of instruction set

```
add     $s1, $a1, $a2
sw      $a1, 0x12 ($a2)
```



14) Using multiple copies of the following diagram, show the active stages for execution of the following sequence of instruction set. Do you see a problem?

add $s1, $a1, $a2

sw $s1, 0x12 ($a2)