EGC442 Problem Set 13 Dr. Izadi

First Name:_____ Last Name: _____

Consider the MIPS datapath of Figure 5.3.5. Find the error in each of the following statements.

1) An R-type instruction like add uses three datapath units: the register file, the ALU, and the data memory.

2) In addition to the register file and ALU, a load or store instruction also involves the sign extension, data memory, and shift left units.

3) The branch datapath uses the sign extension, shift by 2, and data memory units.

4) The mux at the upper right either passes PC + 1 (the normal case), or passes a target address from the instruction (for jumps or branches).

Consider the figure above showing the datapath and control unit in Figure 5.4.5 (labeled as "Control"), and table further above listing control unit output signals.

5) The control unit sends _____ bits to the ALU control.

- 0
- 1
- 2

6) The control unit enables a write to the register file using the _____ signal.

- RegDst
- MemWrite
- RegWrite

7) When MemToReg is 0, the data appearing at the register file's data input comes from the _____.

- ALU's output
- data memory's output
- register file's output

8) The ALU's top input always comes from the Read data 1 output of the register file. The ALU's bottom input can come from two possible places: The Read data 2 output of the register file, or the instruction's lower 16 bits, sign extended to 32 bits. Which control unit output select among those two places?

- ALUOp
- ALUSrc
- Zero

9) The control unit's Branch output will be 1 for a branch equal instruction. However, the branch's target address is only loaded into the PC if the ALU's Zero output is _____. Otherwise, PC is loaded with PC + 4.

- 0
- 1
- (actually, Zero is not involved)

Consider the above Figure 5.4.8 illustrating the datapath in action for a branch equal instruction.

10) The value for the ALUSrc control signal is ____.

- 0
- 1

11) The value for the ALUOp control signal is ____.

- 00
- 01

12) Assume the current instruction is beq $t1, $t2, offset, and $t1 is 90 while $t2 is 85. The value for the Branch control signal is ____.

- 0
- 1

13) Assume the current instruction is beq $t1, $t2, offset, and $t1 is 90 while $t2 is 85. The value for the Zero control signal is ____.

- 0
- 1

14) Assume the current instruction is beq $t1, $t2, offset, and $t1 is 90 while $t2 is 85. How will the PC be updated next?

- PC + 4
- Target address

115) The datapath shown requires four clock cycles to execute a branch instruction.

- True
- False

16) During a branch on equal instruction, two registers are read, those registers' values are subtracted. If the result is 0, Zero becomes 1, causing a new target address to pass through the mux on the upper right and be waiting to enter the PC on the next rising clock edge.

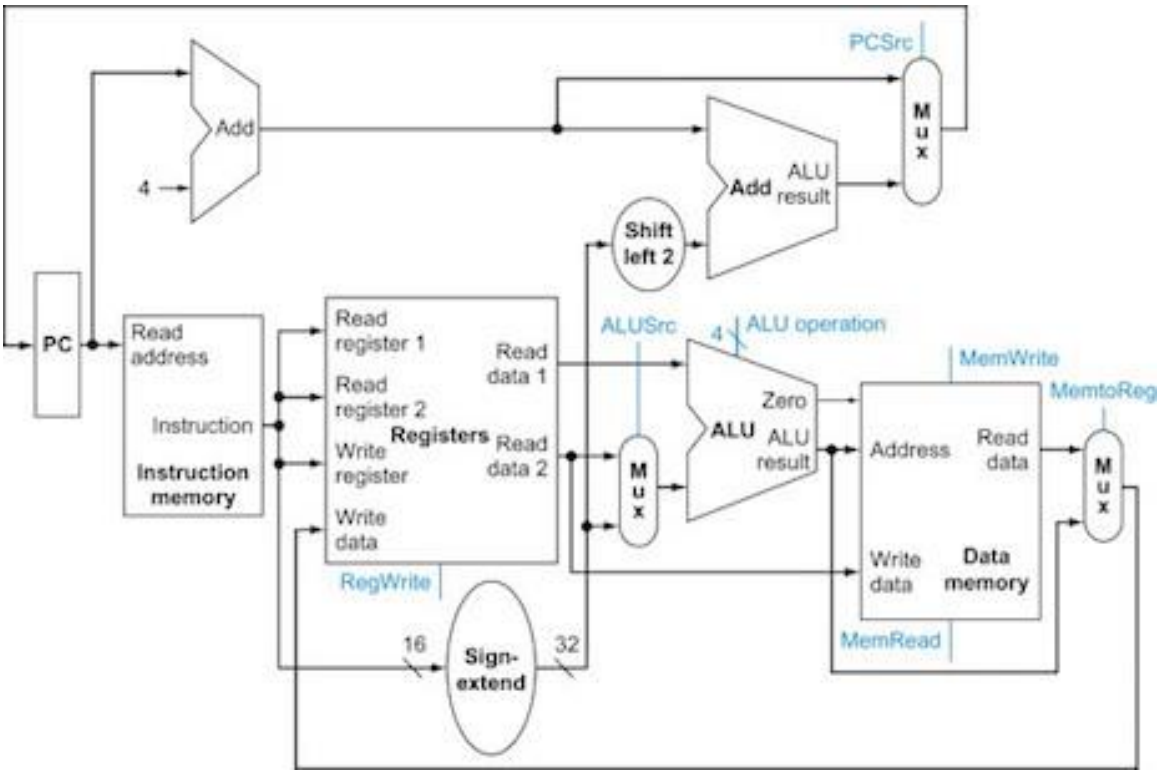
- True
- False

17)

Highlight the active data path for:

- *add* *$4, $5, $6*

Annotate the different segments of highlighted datapath with what they carry Assume the instruction is at memory location 0X1000, ($4) = 0X9 , and ($5) = 0X6000, and ($6) = 0X2040



After execution:

$4 = $5= $6= PC=