EGC442	Problem Set 12	Dr. Izadi
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Consider a rising clock edge that causes 3000 to be written into the PC.

- 1) The 3000 waits at the instruction memory input for the next rising clock edge, at which time the instruction at address 3000 is read out.
- <sup>©</sup> True
- © False

2) After the address 3000 is read into the PC, the 3000 only propagates to the adder.

- © True
- <sup>©</sup> False

3) The 3000 waits at the adder input for the next rising clock edge.

- True
- © False

4) 3001 will be waiting at the PC's input to be written on the next rising clock edge.

- <sup>O</sup> True
- © False

5) The register file always outputs the two registers' values for the two input read addresses.

- <sup>©</sup> True
- © False
  - 6) The register file writes to one register on every rising clock edge.
- <sup>O</sup> True
- © False
  - 7) The design can read from two registers and write to one register during the same clock cycle.
- <sup>©</sup> True
- © False
  - 8) The programmer must take care not to create a program that writes to a register during the same cycle that the same register is read.
- <sub>True</sub>
- © False

9) Consider the MIPS datapath. Find the error in each of the following statements: An R-type instruction like add uses three datapath units: the register file, the ALU, and the data memory.

- 10) Daw the data path for only *lw rt, d16 (rs)*. Make sure to only use the components that are necessary.
- 11) Draw the data path for the following assumed instruction. Make sure to only use the components that are necessary.

*swr* rt, rd (rs);  $\operatorname{Reg}[rt] \rightarrow \operatorname{Mem}[\operatorname{Reg}[rd] + \operatorname{Reg}[rs]]$ 

- 12) Draw the data path for the following instruction set:
  - *lw rt, d16(rs),*
  - *sw rt, d16(rs),*
  - *R-type*,
  - *bne rs,rt, d16,*
  - swr rt, rd(rs)