

First Name: \_\_\_\_\_ Last Name: \_\_\_\_\_

1. Determine the  $g_i$ ,  $p_i$ ,  $P_i$ , and  $G_i$  values of the following two 16 bit numbers. What is  $C_{out15}$  ( $C_{16}$ )?

$$\begin{array}{r} 0001\ 1010\ 0011\ 0011 \\ + \underline{1110\ 0101\ 1110\ 1011} \end{array}$$

$$p_i = a_i + b_i$$

$$g_i = a_i b_i$$

$$c_i$$

Repeat Using  $P_i$  and  $G_i$

$$P_0 = \quad P_1 = \quad P_2 = \quad P_3 =$$

$$G_0 =$$

$$G_1 =$$

$$G_2 =$$

$$G_3 =$$

$$C_4 =$$

2. Assume you are asked to design a 64 bit carry lookahead carry adder as indicated below:
- At the level one, use  $p_i$  and  $g_i$  and  $c_i$ , to express the Boolean function.
  - At the second level use  $P_i$ ,  $G_i$ ,  $C_i$  to express the Boolean function.
  - At the third level use  $P_i'$ ,  $G_i'$ , and  $C_i'$  to express the Boolean function.
3. One simple way to model time for logic is to assume each AND and OR gate takes the same time for a signal to pass through it. Time is estimated by simply counting the number of gates along the longest path through a piece of logic. Compare the number of gate delays for the critical paths of the following 64-bit adders
- Ripple carry
  - three-level carry lookahead
  - Carry lookahead at level one, and ripple carry between 4 bit modules
  - Carry lookahead at levels one and two, and ripple carry between 16 bit modules.