First Name: \_\_\_\_\_ Last Name: \_\_\_\_

1) Add the following numbers using the floating-point addition algorithm. Assume 4 bits of precision.

```
a. 1.010 \times 2^{-3} + 0.011 \times 2^{-3} = ?
```

- 0 1.101
- © 1.101 x 2<sup>-6</sup>
- © 1.101 x 2<sup>-3</sup>

b. 
$$1.001 \times 2^{-4} + 1.000 \times 2^{-6} = ?$$

- $^{\circ}$  10.001 × 2<sup>-4</sup>
- $^{\circ}$  1.011 × 2<sup>-4</sup>

c. 
$$1.000 \times 2^3 + 0.011 \times 2^5 = ?$$

- $0.010 \times 2^4$
- $0.101 \times 2^5$
- $^{\circ}$  10.001 × 2<sup>5</sup>

2. Multiply -14<sub>ten</sub> and -0.25<sub>ten</sub>, or -1.110  $\times$  2<sup>3</sup>  $\times$  -1.000  $\times$  2<sup>-2</sup>. Assume 4 bits of precision.

- 1.110000
- 1.110000<sub>two</sub>  $\times 2^1$
- $1.1100_{\text{two}} \times 2^{1}$
- -
- 3 + (-2) = 1
- 2<sup>1</sup>
- 3.5<sub>ten</sub>

Adding the non-biased exponents of the operands

Multiply the significands:

$$1.110 \times 1.000 = ?$$

Product =  $1.110000 \times ?$ 

Normalize the product

Round the product

Set the sign of the product: ?  $1.1100_{\text{two}} \times 2^1$ 

$$-14_{ten} \times -0.25_{ten} = ?$$

3. Design the least significant a 32 bit ALU with the following functionality.

AND	
OR	
XOR	
ADD	
SUB	
SLT	

4. Design the most significant a 32 bit ALU with the following functionality.

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SLT	

5. Using Verilog design a 32 bit ALU with the following specification. Your code should include indicated flags.

