1) Convert $(32.2)_4$ to base 8.

2) Convert $(1E2.C1)_{16}$ directly base 2.

3) Perform the following operations in the indicated base.

a.

$$\begin{array}{r} (57.4)_8 \\ +(16.5)_8 \\ \hline \end{array}$$

b.

$$\begin{array}{r} (34.3)_6 \\ -(24.5)_6 \\ \hline \end{array}$$

c.

$$\begin{array}{r} (35)_7 \\ \times(5.2)_7 \\ \hline \end{array}$$

4) Perform the following operations in the indicated base.

$$\begin{array}{r} (2.3)_4 \\ \times(2.1)_4 \\ \hline \end{array}$$

5) Using a total of 8 bits, represent -123 in signed 2's complement format.

6) The given numbers are represented in signed 2's complement. Carry out the indicated operation and specify the indicated flags.

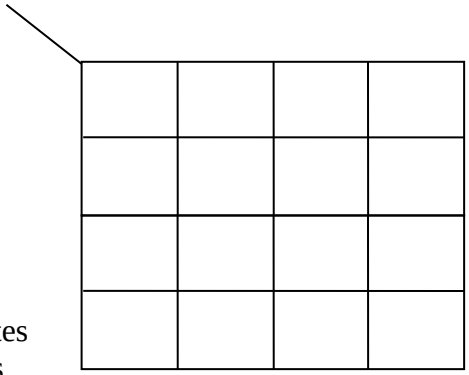
01101011 - 11000010 =

Carry = Sign = Overflow =

7) Determine the following for the given function.

$F = A\overline{C} + \overline{B}D + \overline{A}CD + ABCD$

a. Truth table
b. Sum of min-terms
c. Product of max-terms
d. Standard sum of products
e. Standard product of sums
f. Minimum sum of products
g. Minimum product of sums
h. Circuit implementation using NAND gates
i. Circuit implementation using NOR gates

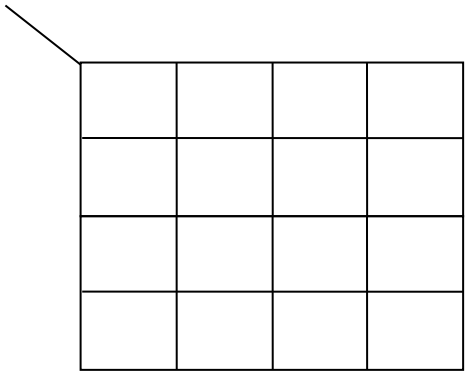


8) Determine the **minimum sum of products** and the **minimum product of sums** of the following.

$F(A,B,C,D)=\Sigma m(0, 2, 4, 5, 8, 14, 15) + d(7, 10, 13)$

Min. S.O.P.

Min. P.O.S.



9) Prove or disprove that the dual of $\overline{A} \oplus B = \overline{A \oplus B}$

10) Show the **truth table only** of a combinational circuit that multiplies two numbers A (A_1A_0) and B (B_1B_0). The range of A is 0 to 2 and the range of B is 1 to 3.

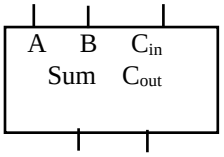
11) Design a 1-out-of-4 decoder with low active outputs and two enable lines, one active high and the other active low. Show the block diagram, the truth table and the internal circuitry.

12) Show the truth table and internal circuitry, Using NAND gates, of an 8 X 1 multiplexer.

13) Using 2 × 1 multiplexers, design an 8 × 1 multiplexer.

14) Using XOR gates and block diagram of full-adders, design a 4-bit adder / subtractor which would function as follows. Justify your answer

Block diagram of one bit full adder →



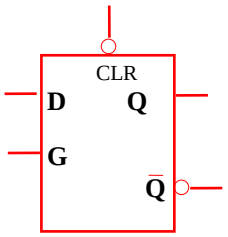
X = 0 →	$R_3R_2R_1R_0 = A_3A_2A_1A_0 + B_3B_2B_1B_0$
X = 1 →	$R_3R_2R_1R_0 = A_3A_2A_1A_0 - B_3B_2B_1B_0$

15) Using gates and multiplexer(s), design a one-bit ALU that performs the following logical operations:

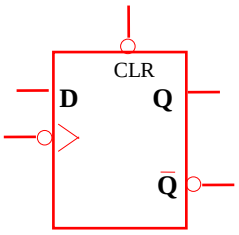
S_1	S_0	Function
0	0	AND
0	1	OR
1	0	XOR
1	1	NOT

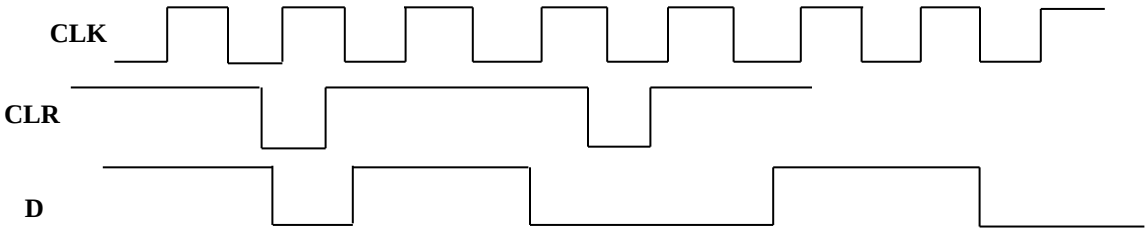
16) Complete the following timing diagram for the given device. Assume Q to be initially 0.

a.



b.





(Part a) **Q**

.....

(Part b) **Q**

.....

16)

a. Using D flip-flop, design an 8-bit register.

b. Using part a as well as other devices such as multiplexers, decoders, and gates, design a register file with 16 8-bit registers such that it can allow reading of any two registers and writing of any one.