EGC442 HW #4 *Dr. Izadi*

First Name: _____ *Last Name:*_____

Problem 1 (30 Points)

Consider the following instruction:

lw rt, d16 (rs)

a. What are the values of control signals generated by the control in COD Figure 4.2 (The basic implementation of the MIPS subset …) for the above instruction?

b. Which resources (blocks) perform a useful function for this instruction?

c. Which resources (blocks) produce outputs, but their outputs are not used for this instruction? Which resources produce no outputs for this instruction?

I. Draw only the data path for the instruction
II. Highlight the active components on a printed copy of

http://www.engr.newpaltz.edu/~bai/EGC442/f519.pdf

Problem 2 (30 Points)

The basic single-cycle MIPS implementation in COD Figure 4.2 (The basic implementation of the MIPS subset …) can only implement some instructions. New instructions can be added to an existing Instruction Set Architecture (ISA), but the decision whether or not to do that depends, among other things, on the cost and complexity the proposed addition introduces into the processor datapath and control. The first three problems in this exercise refer to the new instruction:

Instruction: *swr rt, rd (rs)*

Interpretation: Reg[Rt] => Mem[Reg[Rd] + Reg[Rs]]

a. Which existing blocks (if any) can be used for this instruction?

b. Which new functional blocks (if any) do we need for this instruction?

c. What new signals do we need (if any) from the control unit to support this instruction?

I. Draw only the data path for the instruction
II. Highlight the active components and make your modification on printed copy of http://www.engr.newpaltz.edu/~bai/EGC442/f519.pdf

Problem 3 (20 Points)

When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. In the following three problems, assume that we are starting with a datapath from COD Figure 4.2 (The basic implementation of the MIPS subset …), where I-Mem, Add, Mux, ALU, Regs, D-Mem, and Control blocks have latencies of 400 ps, 100 ps, 30 ps, 120 ps, 200 ps, 350 ps, and 100 ps, respectively, and costs of 1000, 30, 10, 100, 200, 2000, and 500, respectively.

Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we will no longer need to emulate the MUL instruction.

a. What is the clock cycle time with and without this improvement?

b. What is the speedup achieved by adding this improvement?

c. Compare the cost/performance ratio with and without this improvement.

Problem 4 (20 Points)

In this exercise we examine in detail how an instruction is executed in a single-cycle datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word:

10101100011000100000000000010100

Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched:

r0	r1	r2	r3	r4	r5	r6	r8	r12	r31
0	–1	2	–3	–4	10	6	8	2	–16

a. What are the outputs of the sign-extend and the jump "Shift left 2" unit (near the top of COD Figure 4.24 (The simple control and datapath are extended to handle the jump instruction)) for this instruction word?

b. What are the values of the ALU control unit's inputs for this instruction?

c. What is the new PC address after this instruction is executed? Highlight the path through which this value is determined.

d. For each Mux, show the values of its data output during the execution of this instruction and these register values.

e. For the ALU and the two add units, what are their data input values?

f. What are the values of all inputs for the "Registers" unit?

Due 3/24/ 2023