EGC-442 HW #1 Dr. Izadi

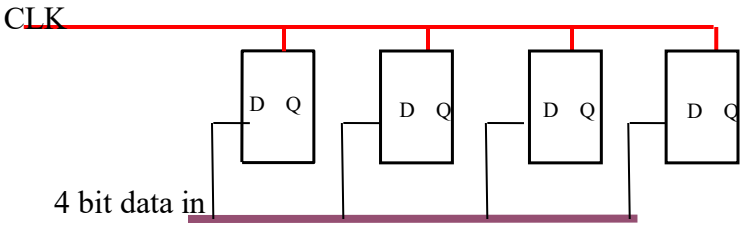
First Name: _____Key_____ Last Name: _____

Question 1 (20 Points)

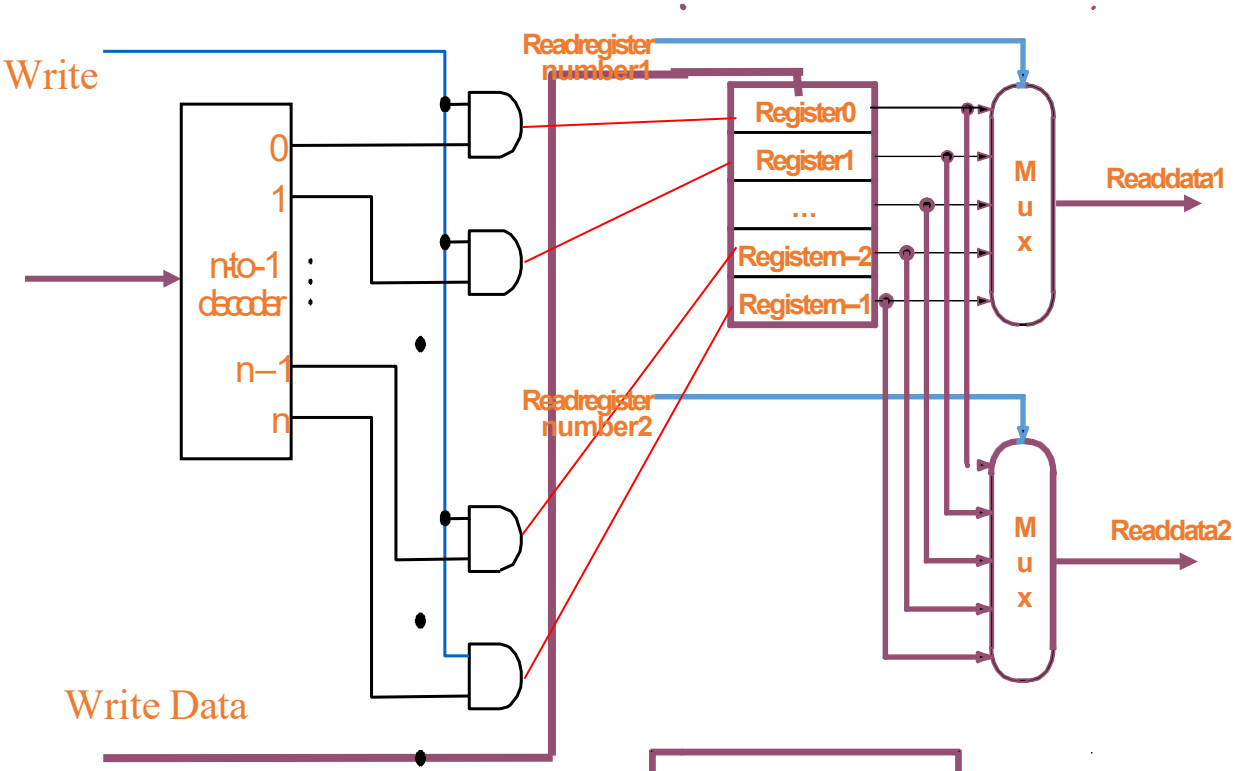
a. Design a 4-bit register. 5 PT)

b. Utilize the block diagram of the 4-bit register from part a along with multiplexers, decoders, and any other needed gates to design a register file with 8 4-bit registers such that it can allow reading of any two registers and writing of any one. (10 PT)

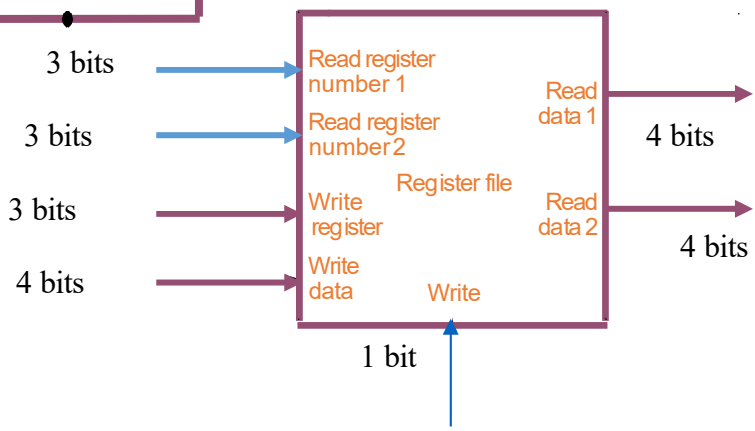
c. n the block diagram similar to below, mark the number bits each line represent.(5 PT)



b.



c.



Question 2.1 (20 Points)
Do problem 1.7 in chapter 2
The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

(a) For each processor find the average capacitive loads.

$C = 2 \times DP/(V^2 \times F)$
Pentium 4: C = 3.2E–8F
Core i5 Ivy Bridge: C = 2.9E–8F

(b) Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

Pentium 4: 10/100 = 10%
Core i5 Ivy Bridge: 30/70 = 42.9%
(c)
If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

$(S_{new} + D_{new})/(S_{old} + D_{old}) = 0.90$
$D_{new} = C \times V_{new}^{\ 2} \times F$
$S_{old} = V_{old} \times I$
$S_{new} = V_{new} \times I$
Therefore:
$V_{new} = [D_{new}/(C \times F)]^{1/2}$
$D_{new} = 0.90 \times (S_{old} + D_{old}) - S_{new}$
$S_{new} = V_{new} \times (S_{old}/V_{old})$
Pentium 4:
$S_{new} = V_{new} \times (10/1.25) = V_{new} \times 8$
$D_{new} = 0.90 \times 100 - V_{new} \times 8 = 90 - V_{new} \times 8$
$V_{new} = [(90 - V_{new} \times 8)/(3.2E\text{-}8 \times 3.6E9)]^{1/2}$
$V_{new} = 0.85V$
Core i5:
$S_{new} = V_{new} \times (30/0.9) = V_{new} \times 33.3$
$D_{new} = 0.90 \times 70 - V_{new} \times 33.3 = 63 - V_{new} \times 33.3$
$V_{new} = [(63 - V_{new} \times 33.3)/(2.9E\text{-}8 \times 3.4E9)]^{1/2}$
$V_{new} = 0.64V$

Question 2.2 (1.7 -2) (20 Points)
Assume for arithmetic, load/store, and branch instructions, a processor has CPIs of 1, 12, and 5, respectively. Also assume that on a single processor a program requires the execution of 2.56E9 arithmetic instructions, 1.28E9 load/store instructions, and 256 million branch instructions. Assume that each processor has a 2 GHz clock frequency.

Assume that, as the program is parallelized to run over multiple cores, the number of arithmetic and load/store instructions per processor is divided by 0.7 x p (where p is the number of processors) but the number of branch instructions per processor remains the same.

(a) Find the total execution time for this program on 1, 2, 4, and 8 processors, and show the relative speedup of the 2, 4, and 8 processor result relative to the single processor result.

P=1:

Total Clock Cycles = $2.56\times10^9 \times1 + 1.28\times10^9 \times12 + .256\times10^9 \times5$
$= 1.92\times10^{10}$
Execution Time = Total Clock Cycles / Clock Frequency
$= 1.92\times10^{10} / 2\times10^9$
$= 9.6$ Sec.
P=2:
Total Clock Cycles =$(2.56\times10^9 \times1 + 1.28\times10^9 \times12)/1.4 + .256\times10^9 \times5$
$= 17.92\times10^9 / 1.4 + 1.28\times10^9$
$= 1.408 \times10^{10}$
Execution Time = Total Clock Cycles / Clock Frequency
$= 1.408 \times10^{10}/2\times10^9$
$= 7.04$ Sec.
Speed up = 9.6 / 7.04 = 1.36

P=4:
Total Clock Cycles =$(2.56\times10^9 \times1 + 1.28\times10^9 \times12)/2.8 + .256\times10^9 \times5$
$= 17.92\times10^9 / 2.8 + 1.28\times10^9$
$= 7.68 \times10^9$
Execution Time = Total Clock Cycles / Clock Frequency
$= 7.68 \times10^9/2\times10^9$
$= 3.84$ Sec.
Speed up = 9.6 / 3.84 = 2.5

P=8:
Total Clock Cycles =$(2.56\times10^9 \times1 + 1.28\times10^9 \times12)/5.6 + .256\times10^9 \times5$
$= 17.92\times10^9 / 5.6 + 1.28\times10^9$
$= 4.48 \times10^9$
Execution Time = Total Clock Cycles / Clock Frequency
$= 4.48 \times10^9/2\times10^9$
$= 2.24$ Sec.
Speed up = 9.6 / 2.24 = 4.285

p	# arith inst.	# L/S inst.	# branch inst.	cycles	ex. time	speedup
1	2.56E9	1.28E9	2.56E8	1.92E10	9.6	1
2	1.83E9	9.14E8	2.56E8	1.408E10	7.04	1.36
4	9.12E8	4.57E8	2.56E8	7.68E9	3.84	2.5
8	4.57E8	2.29E8	2.56E8	4.48E9	2.24	4.285

(b) If the CPI of the arithmetic instructions was doubled, what would the impact be on the execution time of the program on 1, 2, 4, or 8 processors?

P=1:
Execution Time = Total Clock Cycles / Clock Frequency
$= (2.56\times10^9 \times2 + 1.28\times10^9 \times12 + .256\times10^9 \times5)/2\times10^9$
$= 10.88$ Sec.

P=2:Execution Time = Total Clock Cycles / Clock Frequency

$=[((2.56\times10^9 \times2+ 1.28\times10^9 \times12)/1.4) + .256\times10^9 \times5]/2\times10^9$

$= 7.95$ Sec.

P=4: Execution Time = Total Clock Cycles / Clock Frequency

$=[((2.56\times10^9 \times2+ 1.28\times10^9 \times12)/2.8) + .256\times10^9 \times5]/2\times10^9$

$= 4.297$ Sec.

P=8: Execution Time = Total Clock Cycles / Clock Frequency

$=[((2.56\times10^9 \times2+ 1.28\times10^9 \times12)/5.6) + .256\times10^9 \times5]/2\times10^9$

$= 2.469$ Sec.

p	ex. Time
1	10.88
2	7.95
4	4.297
8	2.469

(c) To what should the CPI of load/store instructions be reduced in order for a single processor to match the performance of four processors using the original CPI values?

Since they both have the same clock frequency, we only need to match their number of clock cycles: P=4:

Total Clock Cycles $=(2.56\times10^9 \times1+ 1.28\times10^9 \times12)/2.8 + .256\times10^9 \times5$

$= 17.92\times10^9 /2.8 + 1.28\times10^9$

$= 7.68 \times10^9$

P=1:

Total Clock Cycles $= 2.56\times10^9 \times1+ 1.28\times10^9 \times CPI_{LS} + .256\times10^9 \times5$

$= 7.68 \times10^9$

$CPI_{LS}= 3$

Question 3 (1.8) (15 Points)

When a program is adapted to run on multiple processors in a multiprocessor system, the execution time on each processor is comprised of computing time and the overhead time required for locked critical sections and/or to send data from one processor to another.

Assume a program requires t = 100 s of execution time on one processor. When run p processors, each processor requires t/p s, as well as an additional 4 s of overhead, irrespective of the number of processors. Compute the per-processor execution time for 2, 4, 8, 16, 32, 64, and 128 processors. For each case, list the corresponding speedup relative to a single processor and the ratio between actual speedup versus ideal speedup (speedup if there was no overhead).

processors	exec. time/processor	time w/ overhead	speedup	actual speedup/ideal speedup
1	100			
2	50	54	100/54 = 1.85	1.85/2 = .93
4	25	29	100/29 = 3.44	3.44/4 = 0.86
8	12.5	16.5	100/16.5 = 6.06	6.06/8 = 0.75
16	6.25	10.25	100/10.25 = 9.76	9.76/16 = 0.61

Question 4 (20 Points)

Consider two machines A and B. Machine A does not have floating point hardware and implements floating point instruction in software. It takes 20 and 40 Integer instructions to implement a floating point add (FADD) instruction and a floating point Divide (FDIV) instruction, respectively, on machine A. Machine B, on the other hand, has floating point hardware to directly execute FADD and FDIV. An integer instruction executes in one clock cycle on both machines, and FADD and FDIV execute in 3 and 6 clock cycles, respectively, on machine B. Consider a program which has 100 million instructions and the following mi× of instructions:

- 10% FDIV
- 30% FADD
- 60% Integer instructions

a How many clock cycles will it take to execute the program on each of machines A and B?

b How long will it take to execute the program on each of machines A and B, assuming 1 GHz (1000 MHz) clock rate.

c How many native instructions will each machine execute? A native instruction is one that executes directly on the hardware. Note that machine A does not execute FDIV and FADD directly on the hardware, but rather executes 20 native instructions for each FADD and 40 native instructions for each FDIV.

d Compute MIPS rating (the number of million native instructions executing per second) for each machine.

a. (5PT)

CPI of Machine A:

Instruction	*Frequency*	*CPI*	*CPI * Frequency*
FDIV	*0.10*	*40*	*4*
FADD	*0.30*	*20*	*6*
Integer Instr.	*0.6*	*1*	*0.6*
		TOTAL	***10.6***

*Number of Clock CyclesMACHINE A = 100 * 10^6 *10.6 =10.6 *10^8*

*cycles CPI of Machine B= 100 * 10^6 *2.25= 2.25*10^8 cycle*

Instruction	Frequency	CPI	CPI * Frequency
FDIV	0.10	6	.6
FADD	0.30	3	.9
Integer Instr.	0.6	1	0.6
		TOTAL	**2.1**

b. (5PT)

EXecution Time = Number of clock cycles* Cycle Time

EXecution timeMACHINE A = $10.6 * 10^8 / (10^9) = 1.06$ seconds

EXecution timeMACHINE B = $2.1 * 10^8 / (10^9) = 0.21$ seconds

b. (5PT)

Either of Machine A answers are acceptable:

Machine A

Number of Native Instructions = $100 * 10^6 (0.1 * 40 + 0.3 * 30 + 0.6 * 1) = 13.6 * 10^8$ native instructions.

Or

Number of Native Instructions = $100 * 10^6 (0.15 * 40 + 0.25 * 20 + 0.6 * 1) = 10.6 * 10^8$ native instructions.

Machine B

(All instructions are native instructions)

Number of Native Instructions = $100 * 10^6 (1) = 10^8$ native instructions.

c. (5PT)

MIPS = (Number of Native Instructions / EXecution Time for these instructions) / 10^6

Either of machine A answers are acceptable

MIPSMACHINE A = $13.6 * 10^8 / (1.06 * 10^6) = 1283$ MIPS

or

MIPS MACHINE A = $10.6 * 10^8 / (1.06 * 10^6) = 1000$ MIPS

MIPS MACHINE B = $10^8 / (0.21 * 10^6) = 476$ MIPS