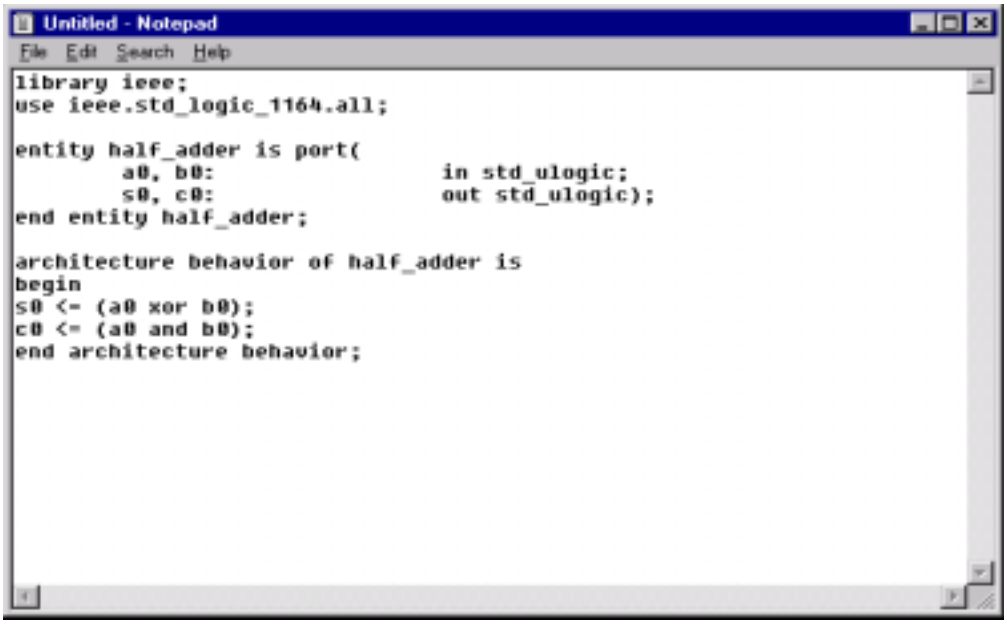
45208 Digital Logic Laboratory
Professor M. Otis

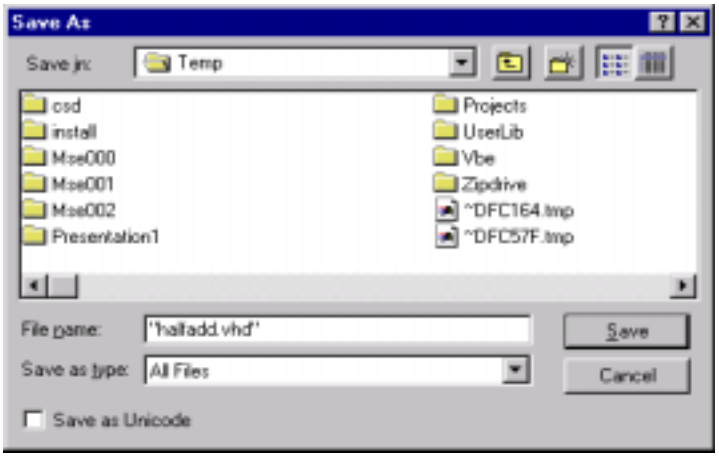
Introduction to VHDL / Synthesis / Fitting / Functional Simulation using Cypress Semiconductor's WARP design environment.

The following document is a tutorial to be used for synthesizing and fitting a design to a SPLD. It utilizes Microsoft's Notepad software for text editing and Cypress' WARP software for synthesis, fitting, and simulation of a simple logic design (half adder circuit).

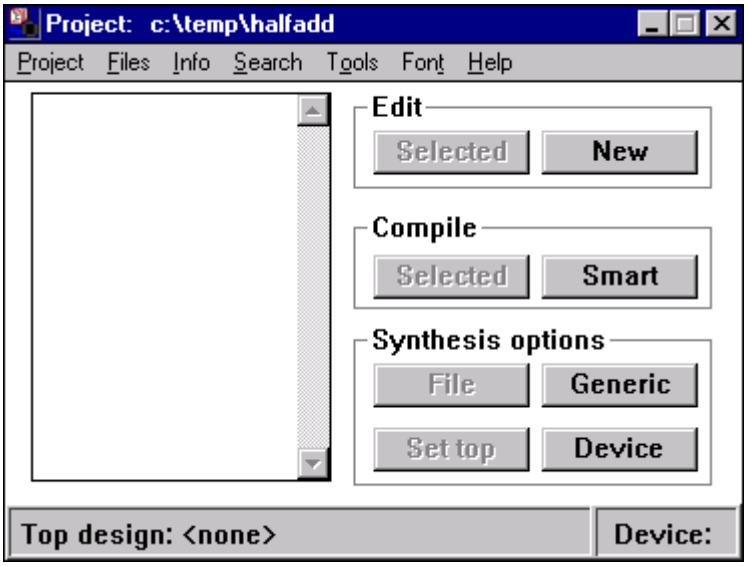
Step 1 of this tutorial is to open up your favorite editor and type the following:



Once completed save as halfadd.vhd in the Temp directory.

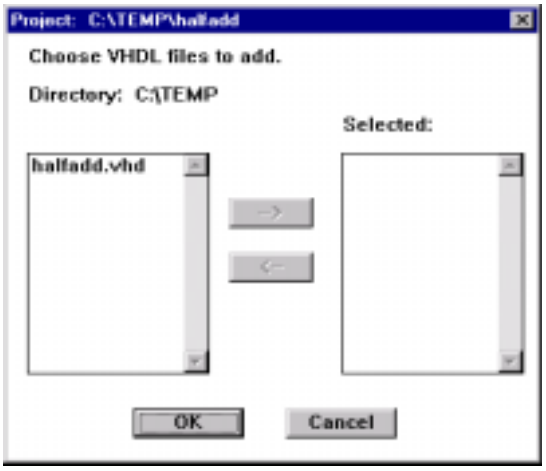


Step 2 - Open up WARP's Galaxy Project tool:

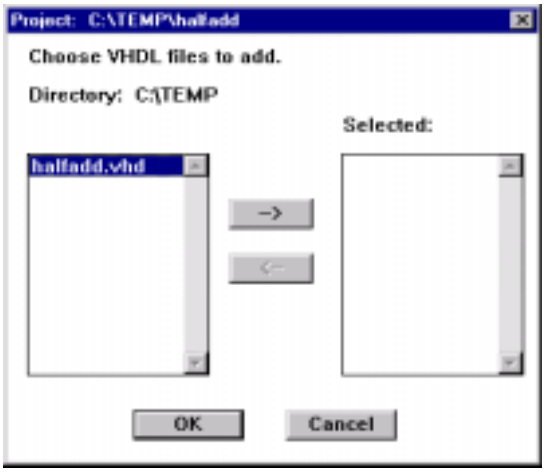


Click on **Project**, and begin a **New** project.

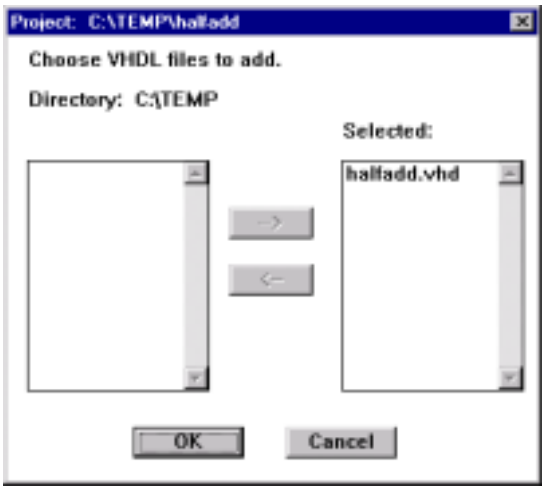
Step 3 - From the **File** menu, select **Add**. You should see halfadd.vhd on the left.



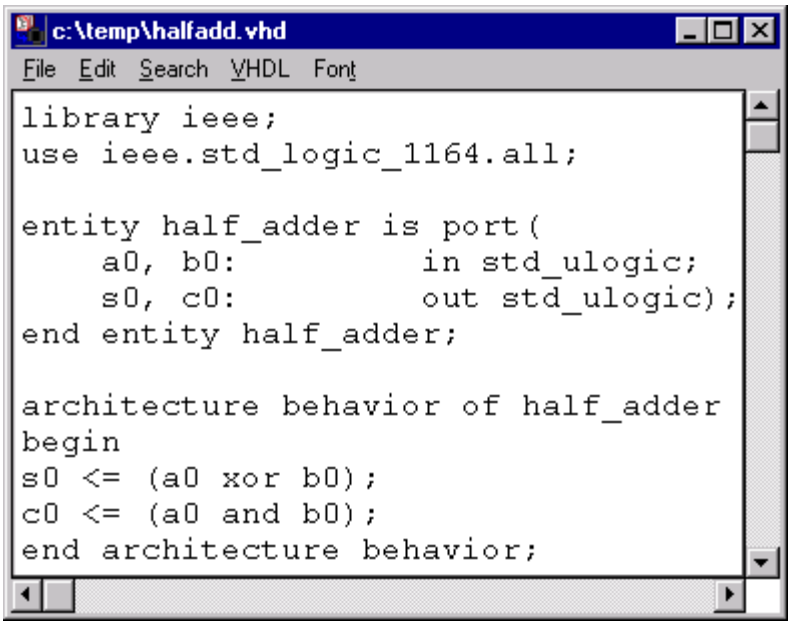
Click on halfadd.vhd to highlight it.



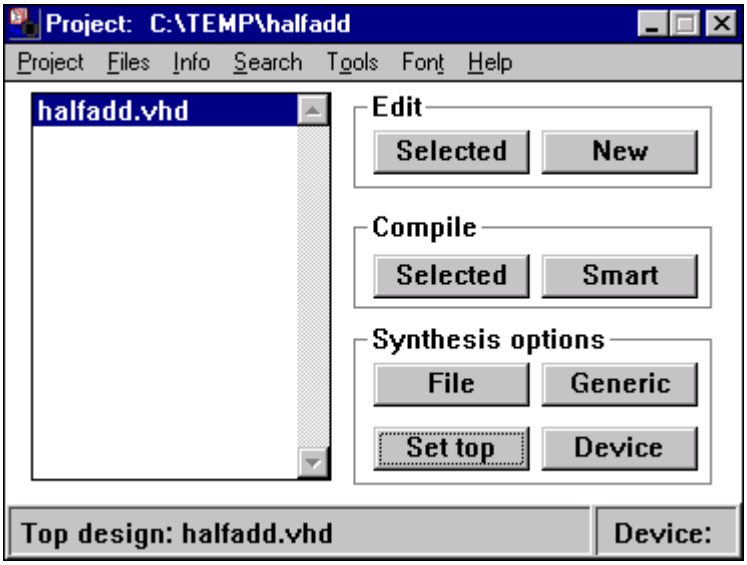
Move halfadd.vhd to the Selected box.



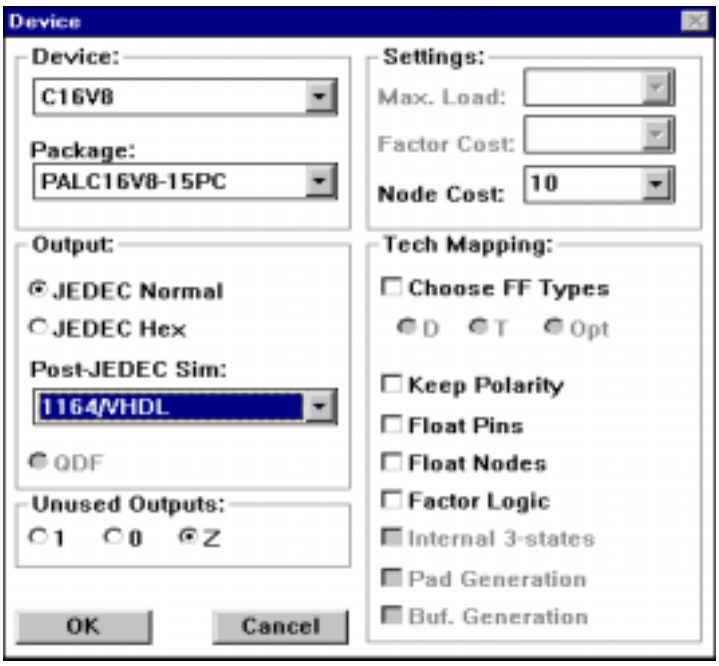
Step 4 - You can verify the selected vhdl code by clicking on **Selected** from the **Edit** panel. Once verified you should close this editor.



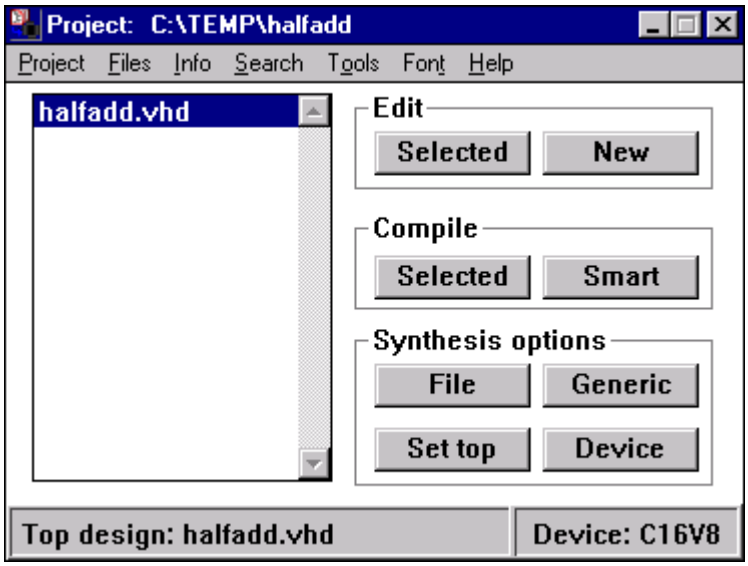
Step 5 - Back at the project box, click on **Set top** in the **Synthesis options** panel.



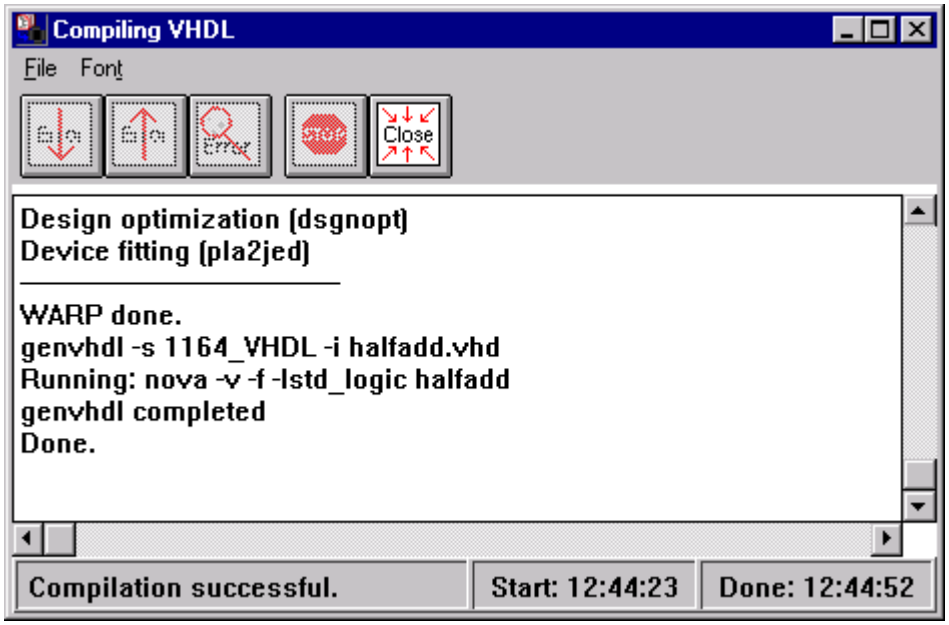
Step 6 - Next click on **Device** in the **Synthesis options** panel. This will invoke the Device dialog box. Edit this box exactly as shown below.



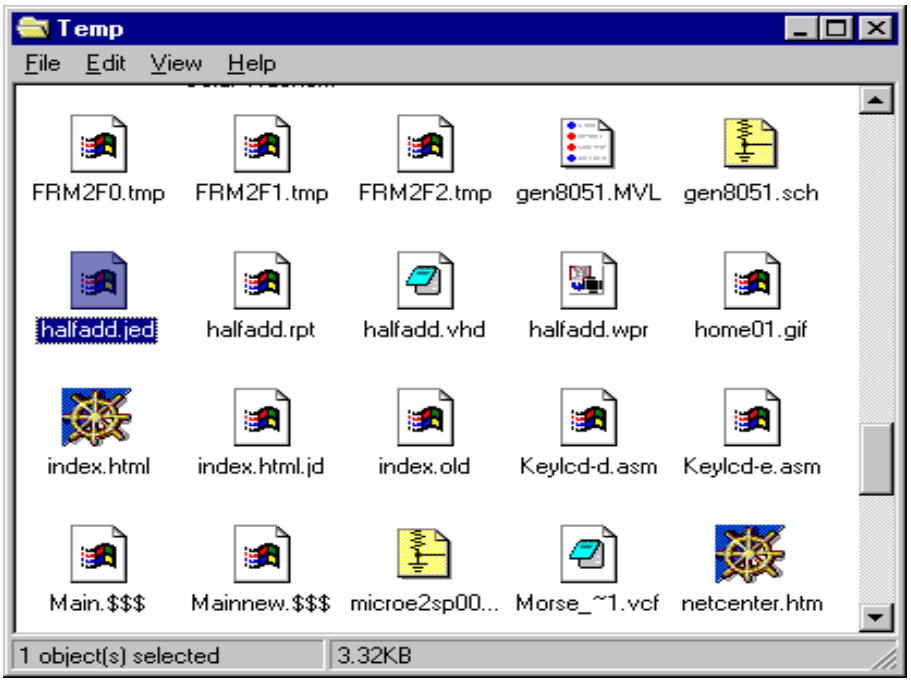
Click OK and the Project GUI should appear as follows.



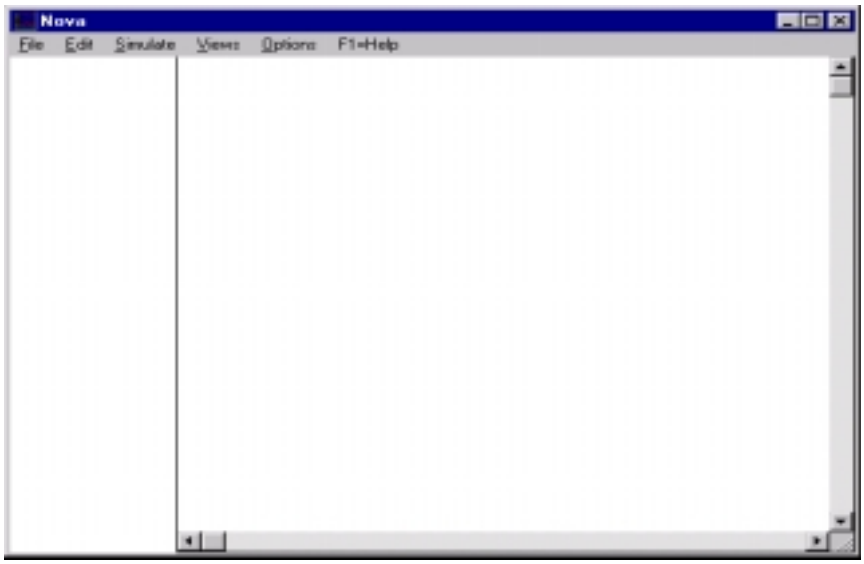
Step 7 - Click on the **Smart** button from the **Compile** menu. The VHDL file will begin to compile, creating a JEDEC file that will be used to download into a SPLD. When complete click on **File**, then **Close**.



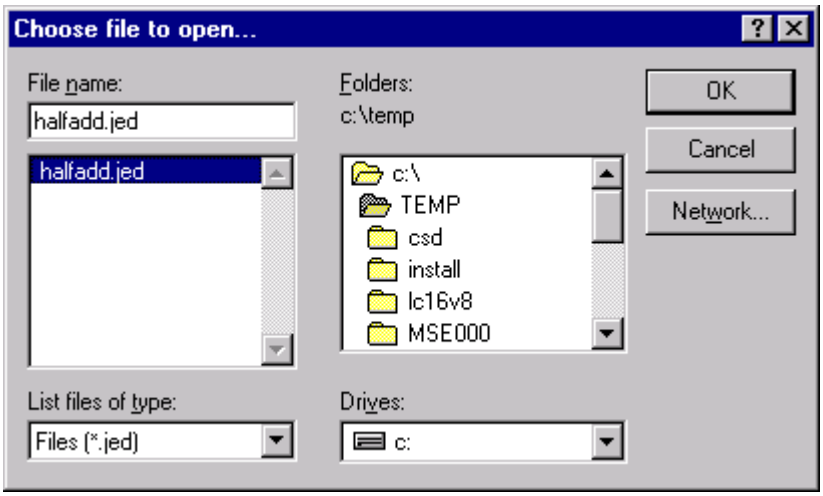
You should verify that your Jedec file exists.



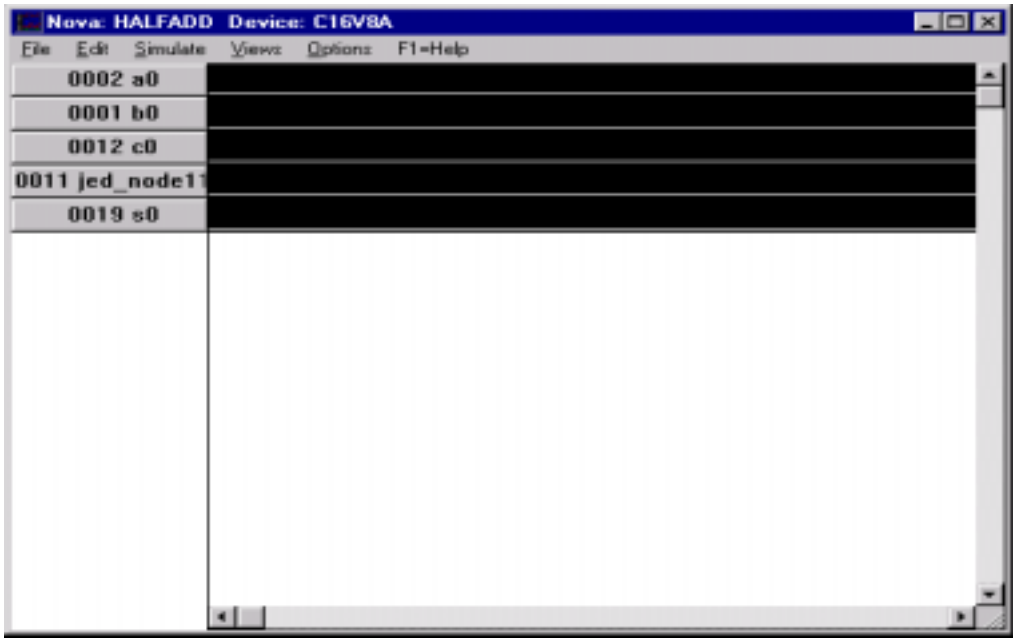
Step 8 - From the **Tools** menu, select **Nova** to start the functional simulator.



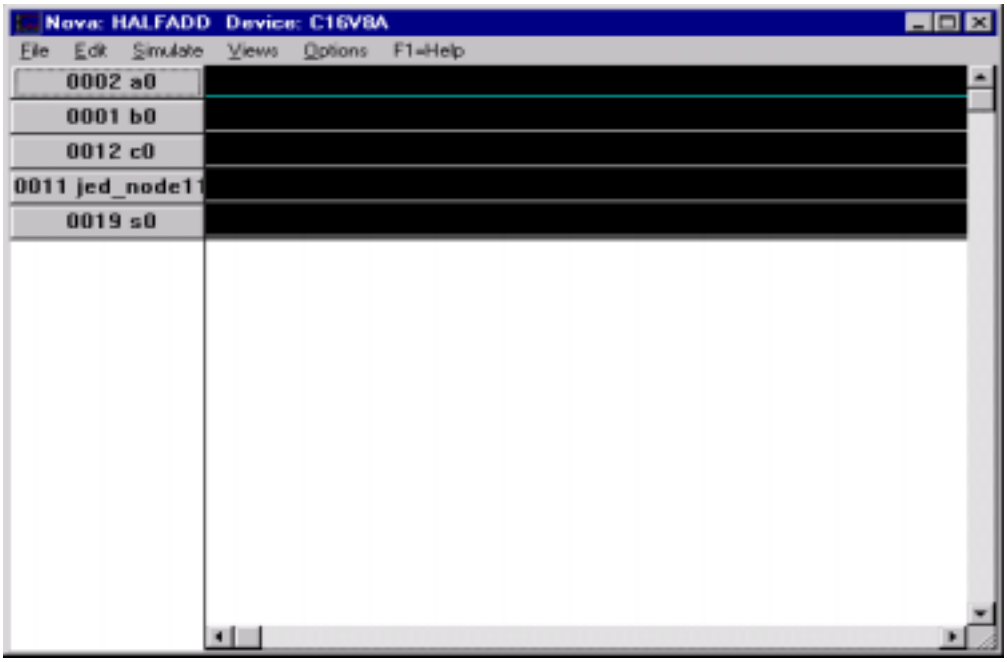
Step 9 - Once in Nova, select **Open** from the **File** menu. Choose halfadd.jed as the file to simulate.



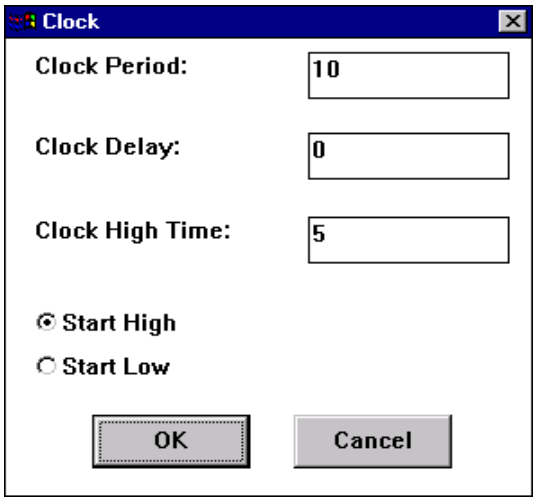
Step 10 - The Nova simulator should appear as follows.



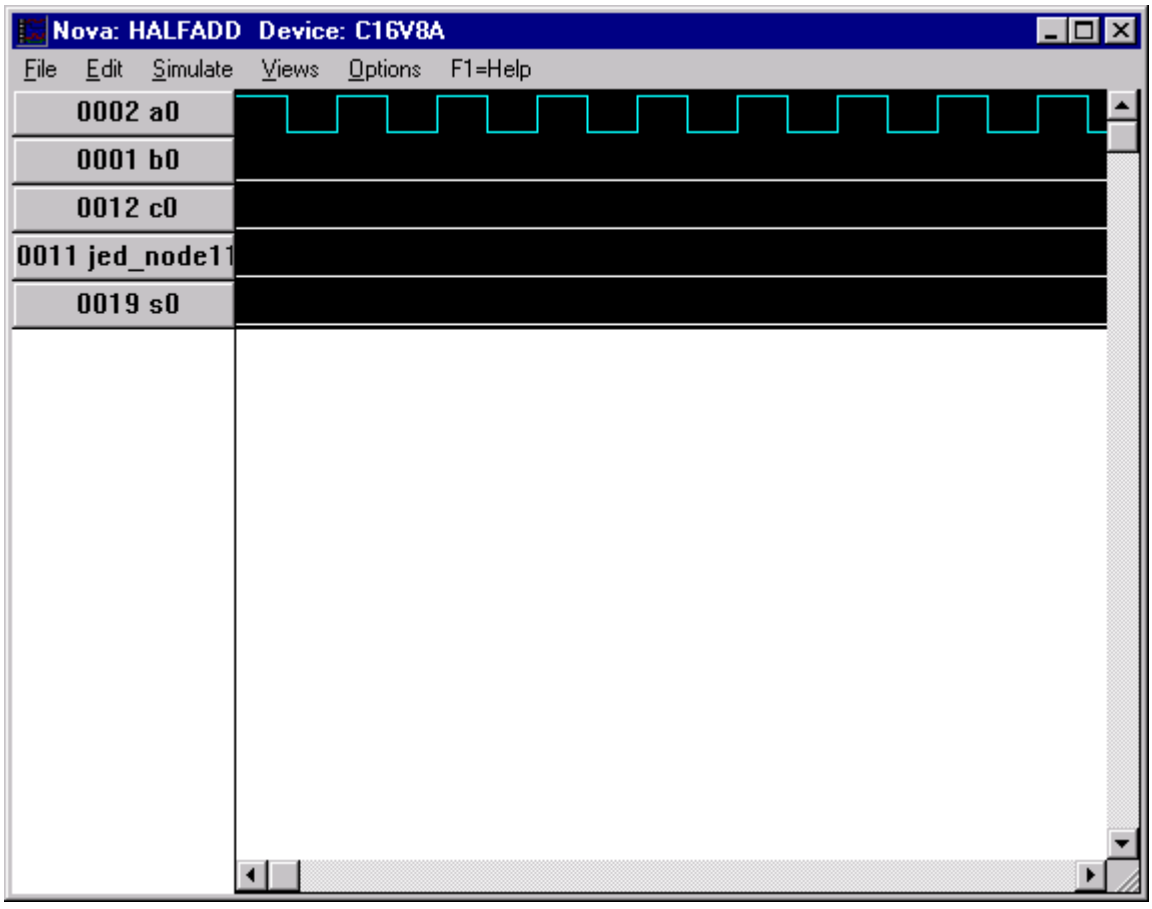
Next you will modify the input stimulus by highlighting an input as shown.



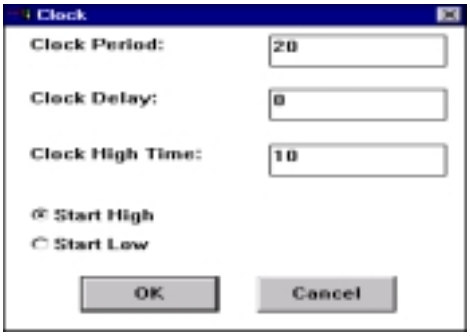
Step 11 - Modify the stimulus by selecting **Clock** from the **Edit** menu. Edit if necessary to provide the same signals as shown below.

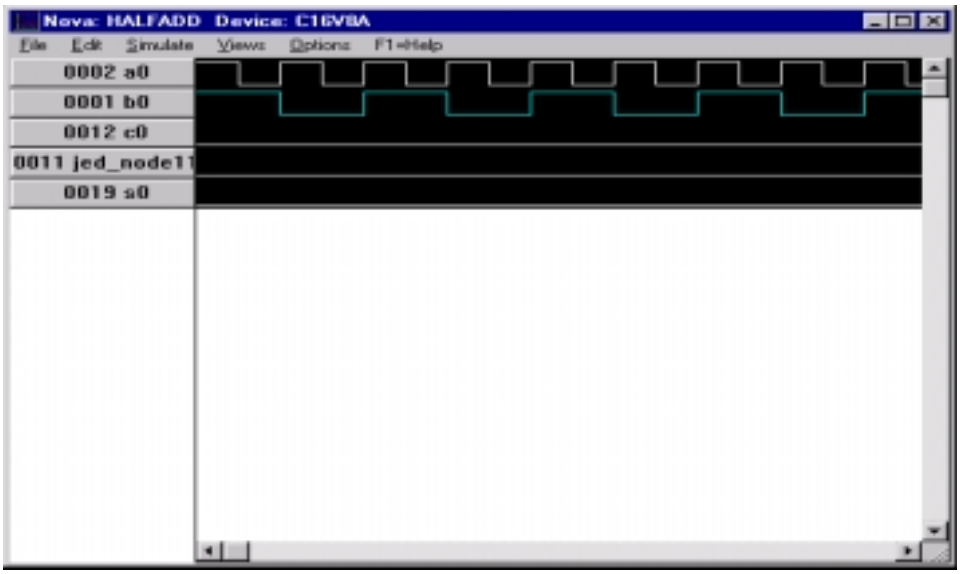


Verify the trace by selecting **OK** and then view the simulator as shown below.

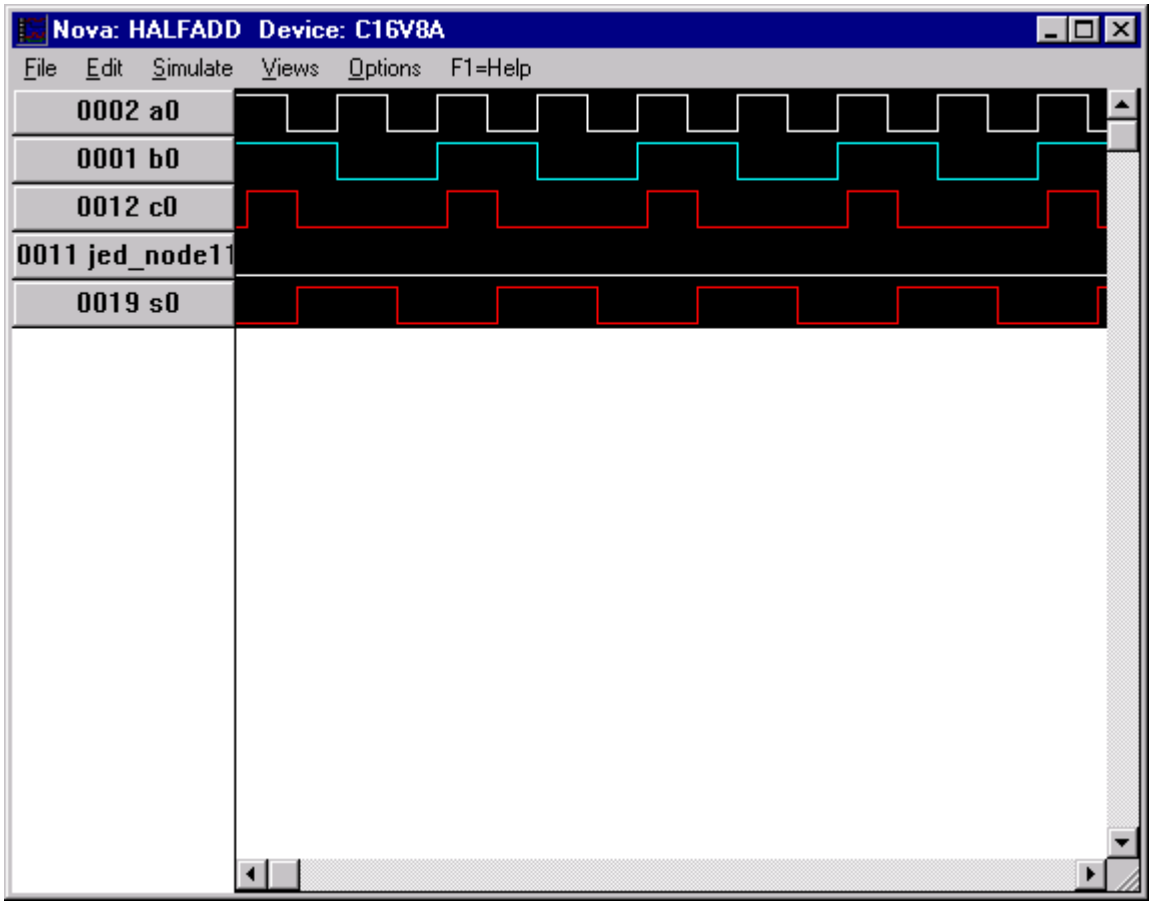


Modify the next input signal using the same methods.





Step 12 - From the **Simulate** pulldown menu, select **Execute**. This will provide you with output traces as shown below. Verify these logic waveforms for accuracy as compared to expected results.



If the simulation is satisfactory, you are now ready to "Burn" your SPLD!

When finished be sure to Exit and Save your project.