45208 Digital Logic Laboratory Professor M. Otis

Introduction to VHDL / Synthesis / Fitting / Functional Simulation using Cypress Semiconductor's WARP design environment.

The following document is a tutorial to be used for synthesizing and fitting a design to a SPLD. It utilizes Microsoft's Notepad software for text editing and Cypress' WARP software for synthesis, fitting, and simulation of a simple logic design (half adder circuit).

Step 1 of this tutorial is to open up your favorite editor and type the following:

Untitled - Notepad		_ D ×
<u>File Edit Search Help</u>		
library ieee; use ieee.std_logic_1164.all;		14
entity half_adder is port(a0, b0: s0, c0: end entity half_adder;	in std_ulogic; out std_ulogic);	
architecture behavior of half_a begin s0 <- (a0 xor b0); c0 <= (a0 and b0);	adder is	
end architecture behavior;		
		<u> </u>
		- 16

Once completed save as halfadd.vhd in the Temp directory.

Save As	? ×
Savejn: 🤤 Temp	• 🗈 🗗 🏢 🏢
Cod Cod	Projects
install	UterLib
Mae000	Vbe
Mae001	Zipdrive
Mae002	 *DFC164.tmp
Presentation1	 DFC57F.tmp
•	•
File pame: ['halfadd.vhd'	Save
Save as type: All Files	Cancel
Save as Unicode	

Step 2 - Open up WARP's Galaxy Project tool:

🌯 Proj	ect: c	::\tem	p\halfad	d			
Project	<u>F</u> iles	<u>I</u> nfo	<u>S</u> earch	T <u>o</u> ols	Font	<u>H</u> elp	
			<u></u>		dit Sele	cted	New
					ompi Sele		Smart
				S.	-		ptions
					Fi	le	Generic
			-		Set	top	Device
Top d	esigr	n: <no< td=""><td>one></td><td></td><td></td><td></td><td>Device:</td></no<>	one>				Device:

Click on **Project**, and begin a **New** project.

×
Creating a new Galaxy
Name:
c:\temp\halfadd
Browse OK Cancel

Step 3 - From the File menu, select Add. You should see halfadd.vhd on the left.

Project: C:\TEMP\halladd	×
Choose VHDL files to add.	
Directory: C:\TEMP	
	Selected:
halfadd.vhd 📧	×
->	
<	
w.	w1
OK	ancel

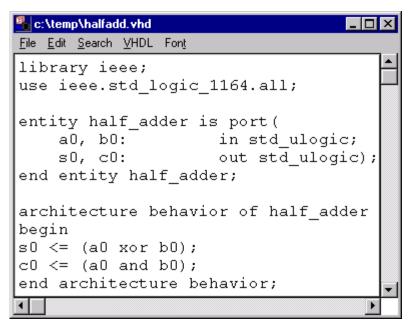
Click on halfadd.vhd to highlight it.

Project: C:\TEMP\halladd	×
Choose VHDL files to add.	
Directory: C:\TEMP	
	Selected:
halfadd.vhd	×
->	
<u>1</u>	×
OK Ca	ncel

Move halfadd.vhd to the Selected box.

Project: C:\TEMP\halfadd		×
Choose VHDL files to add.		
Directory: C:\TEMP		
	Selected:	
->	halfadd.vhd	×
W.		14
OK	ncel	

Step 4 - You can verify the selected vhdl code by clicking on **Selected** from the **Edit** panel. Once verified you should close this editor.



Step 5 - Back at the project box, click on **Set top** in the **Synthesis options** panel.

Project: C:\TEMP\halfadd	_ 🗆 X
<u>Project Files I</u> nfo <u>S</u> earch T <u>o</u>	ols Fon <u>t H</u> elp
halfadd.vhd	Edit Selected New Compile Selected Smart Synthesis options File Generic Set top Device
Top design: halfadd.vhd	Device:

Step 6 - Next click on **Device** in the **Synthesis options** panel. This will invoke the Device dialog box. Edit this box exactly as shown below.

Device	×
Device: C16V8	Settings: Max. Load:
Package: PALC16V8-15PC •	Factor Cost:
Output:	Tech Mapping:
JEDEC Normal	Choose FF Types
C JEDEC Hex	ep er eopt
Post-JEDEC Sim:	C Keep Polarity
1164/VHDL	Float Pins
C QDF	Float Nodes
Unused Outputs:	Factor Logic
01 00 @Z	Internal 3-states
	Pad Generation
OK Cancel	Buf. Generation

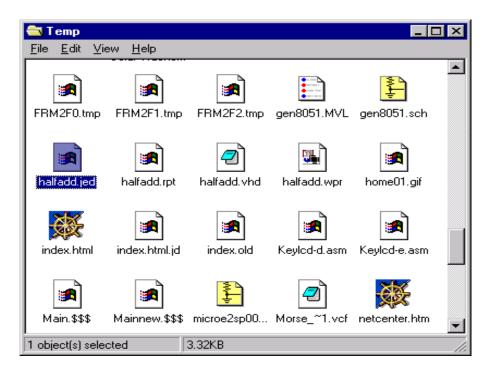
Click OK and the Project GUI should appear as follows.

Project: C:\TEMP\h	alfadd	
<u>Project Files Info Sear</u>	ch T <u>o</u> ols Fon <u>t H</u>	<u>l</u> elp
halfadd.vhd	Edit Selecto	ed New
	Compile	ed Smart
	Synthesi	is options Generic
	Set to	
Top design: halfadd.	vhd	Device: C16V8

Step 7 - Click on the **Smart** button from the **Compile** menu. The VHDL file will begin to compile, creating a JEDEC file that will be used to download into a SPLD. When complete click on **File**, then **Close**.

Compiling VHDL Eile Font Eile Font Eile Font Eile Font		
Design optimization (dsgnopt) Device fitting (pla2jed) WARP done. genvhdl -s 1164_VHDL -i halfadd.v Running: nova -v -f -lstd_logic halfa genvhdl completed Done.		
Compilation successful.	Start: 12:44:23	Done: 12:44:52

You should verify that your Jedec file exists.



Step 8 - From the **Tools** menu, select **Nova** to start the functional simulator.

	ova							- 0 2
Elle	Edit	Simulate	Views	<u>○</u> ptions	F1=Help			
			•					

Step 9 - Once in Nova, select **Open** from the **File** menu. Choose halfadd.jed as the file to simulate.

Choose file to open		? ×
File <u>n</u> ame: halfadd.jed	Eolders: c:\temp c:\ TEMP c:d c:d install lc16v8 MSE000	OK Cancel Network
List files of <u>type:</u> Files (*.jed)	Dri <u>v</u> es: C:	×

	ova: H	ALFADD	Device	: C16V8/	۱.			_ 🗆 ×
Eie	Edit	Simulate	⊻іениз	Options	F1=Help			
	0002	a0						-
	0001	b0						
	0012	cO						
001	1 jed_	node11						
	0019	s0						
			•					- PĒ

Step 10 - The Nova simulator should appear as follows.

Next you will modify the input stimulus by highlighting an input as shown.

		IALFADD						_ 0 ×
Ele		Simulate	⊻iews	<u>Options</u>	F1=Help			
	0002							-
	0001	ь0						_
	0012	c0						
001	1 jed_	node11						
	0019	sO						
								×
			•			 	 	

Step 11 - Modify the stimulus by selecting **Clock** from the **Edit** menu. Edit if necessary to provide the same signals as shown below.

Clock	×
Clock Period:	10
Clock Delay:	0
Clock High Time:	5
⊙ Start High	
C Start Low	
ОК	Cancel

Verify the trace by selecting **OK** and then view the simulator as shown below.

	lova: H	IALFADD	Device	: C16V8/	۱			- 🗆 ×
<u>F</u> ile	<u>E</u> dit	<u>S</u> imulate	⊻iews	<u>O</u> ptions	F1=Help			
	0002	a0						
	0001	b0						
	0012	c0						
001	1 jed_	node11						
	0019	sO						
			•					

	lova: H	ALFADD	Device	C16V8A					×
Ele		Simulate	Views	Options	F1=Help				
	0002	a0							4
	0001	b0							
	0012	c0							
001	1 jed_	node11							
	0019	s0							
			•						-
				_		 	_	 -	222

Modify the next input signal using the same methods.

=1 Clock	
Clock Period:	20
Clock Delay:	0
Clock High Time:	10
I Start High C Start Low	
OK	Cancel

	lova: H	ALFADD	D Device: C16V8A	×
Eile	Edit	≦inulate		
	0002	a0 [4
	0001	bO		7
	0012	c0		
001	1 jed_	node11		
	0019	s0		
			NI 21	믝

Step 12 - From the **Simulate** pulldown menu, select **Execute**. This will provide you with output traces as shown below. Verify these logic waveforms for accuracy as compared to expected results.

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<u>F</u> ile		<u>S</u> imulate	⊻iews	<u>O</u> ptions	F1=Help			
	0002	a0						╵╴╴╻╧
	0001	b0						
	0012	cO						
001	1 jed_	node11						
	0019	sO						
								-
			•			 	 	

If the simulation is satisfactory, you are now ready to "Burn" your SPLD!

When finished be sure to Exit and Save your project.