

**EGC208 Digital Logic Laboratory (1 credits)**  
**Fall 2013 Semester**

**Instructor:** Dr. Baback Izadi, 102 Resnick Engineering Hall  
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<http://www.engr.newpaltz.edu/~bai>

**Course web page:** [http://www.engr.newpaltz.edu/~bai/EGC208/EGC208\\_spring.htm](http://www.engr.newpaltz.edu/~bai/EGC208/EGC208_spring.htm)

**Lecture:** Wednesday 10:50 AM – 1:30 PM, REH211

**Office Hours:** Tuesday 1:30 PM – 2:30 PM  
Wednesday 2:00 PM – 3:30 PM  
Friday 1:30 AM – 3:00 PM  
And by appointment

**Co-requisites:** Digital Logic Fundamentals (EGC230)

**Course catalog description:** Experiments in both combinational and sequential logic circuits - BCD to 7-segment display decoders, full adder, adder-subtractor, and arithmetic and logic unit (ALU). Verilog implementation. Synchronous sequential circuits using D flip-flops, counter designs. This lab uses software tools such as Electronic WorkBench and Xilinx ISE. Designs are finally downloaded into FPGA boards.

**Course Learning Outcomes (LO's):**

- I. Students will learn digital design principles and practices and implement large-scale digital systems, which incorporate digital devices at all complexity levels.
- II. Students will utilize state-of-the-art design entry tools such as schematic capture and Verilog to design and implement their circuits in Field Programmable Gate Arrays.
- III. Students will work in teams to design, simulate, and implement digital circuits.

**Course Contribution to Student Outcomes:**

This lab contributes to our program outcomes as specified in the following table:

<b>Student Outcome</b>	<b>Contributed Learning Outcome</b>	<b>Level of Contribution</b> 3 /3 = strong; 2/3 = moderate; 1/3 = marginal
a) An ability to apply knowledge of mathematics, science and engineering	I	2/3
b) An ability to design and conduct experiments, as well as to analyze and interpret data.	II	3/3
d) An ability to function on multidisciplinary teams.	III	3/3
k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	II	3/3

\* ABET: Accreditation Board for Engineering and Technology

**Design Team:**

Teams of two students will complete each lab as a unit. Team members must be active in all phases of the lab. Inactive team member can be removed at the discretion of other team member or the instructor. Inactivity of team members should be brought to the attention of the instructor. Please note that **attendance is compulsory.**

**General Instructions:**

All materials related to the lab will be available on course website

([http://www.engr.newpaltz.edu/~bai/CSE45208/EGC208\\_spring.htm](http://www.engr.newpaltz.edu/~bai/CSE45208/EGC208_spring.htm).) The students should review the lab prior to the scheduled lab period and be prepared for the lab. A brief overview of the lab experiment will be given at the beginning of each new lab session.

Each student must keep a separate lab notebook, and record all their work (preparatory work and all their observations during the lab session) in it. Each lab should begin on a new page (with no pages left blank) and should include the Title of the lab, Experiment #, and the Date.

Once the lab is completed, the teaching assistant or the instructor will sign off both the cover sheet and the notebook.

The lab notebook must be available for inspection by the instructor and /or TA. It will be reviewed periodically and will be graded. You need to turn in your lab notebook at the end of the semester for grading.

**Lab Report Guidelines:**

A final report (only one report per team) is to be turned in for each lab. You should use a word processor and CAD tools to professionally document your work. The report should have the following sections:

- ◆ Departmental cover sheet (use standard template, a copy can be found at: [http://www.engr.newpaltz.edu/~bai/CSE45208/EGC208\\_fall.htm](http://www.engr.newpaltz.edu/~bai/CSE45208/EGC208_fall.htm)) indicating title of the Lab, course name and number, date (semester and year), and the name of each team member.
- ◆ Table of contents.
- ◆ Introduction – A brief introduction to the topic, and the experiment being carried out.
- ◆ Procedure - all design steps should be documented including the truth table, state table, state diagram, Karnaugh maps, circuitry, etc.
- ◆ Simulation results if needed.
- ◆ Conclusion (problems encountered, lessons learned, etc.).
- ◆ References

Your report should be free of grammatical and spelling errors. Your lab report should reflect only your team's work. If unreasonable similarities are recognized between the turned in reports, they will receive failing grades.

**Assignments:**

Assignments will be posted on the course web site:

[http://www.engr.newpaltz.edu/~bai/CSE45208/EGC208\\_fall.htm](http://www.engr.newpaltz.edu/~bai/CSE45208/EGC208_fall.htm)

Tentative lab schedules are as follows:

Lab number	Title
1	Introduction
2	A 4-bit Adder
3	Design of a Combinational Logic Circuit
4	Design of Full Adder
5	Design of Multiplexer/Demultiplexer
6	Design of a Seven Segment Display
7	Design of an Adder/Subtractor unit
8	Design of a four-bit ALU using Xilinx
9	Verilog implementation of a four-bit ALU using Xilinx
10	Design of a state machine using Xilinx

**Grading Policy:**

Category	Weights
Completed lab notebook with 100% of labs signed off (partially completed lab notebook with at least 70% of labs (4 labs) signed off	15% (10%)
Presentation	5%
Formal lab report:	70%
Attendance	10%
Total:	100%

Each lab report is graded on a 0-10 point scale. A report without a signature is graded on a 0-5 point scale.

**Presentation:**

Each team is expected to make a Power Point presentation of 10 to 15 minutes on the last day of lab. You may consult with me and choose one of the labs. Your presentation should include your design problem and your solution at the appropriate detail. You should conclude with encountered problems and lesson learned.

**Relevant Web Sites:**

- Digital Logic Fundamentals: [http://www.williamson-labs.com/480\\_logic.htm](http://www.williamson-labs.com/480_logic.htm)
- Digital logic tutorial: <http://www.play-hookey.com/digital/>
- Combinational Logic Tutorial:  
<http://www.ee.surrey.ac.uk/Projects/Labview/combindex.html>
- Latches and Flip flops: <http://vorlon.cwru.edu/~jackie/eces301/hw/HW2/lab2.html>
- Texas Instruments Digital Logic Families:  
<http://focus.ti.com/docs/logic/logichomepage.jhtml>

- To download a demo version of Electronic Workbench click on <http://www.interactiv.com/html/demo.html>
- Xilinx: <http://www.xilinx.com/programs/xds1.htm>
- If you need software to view and print PDF files under Windows: <http://www.adobe.com/products/acrobat/readstep.html>

### **Rules and general comments:**

- ◆ Attendance policy: I strongly advise against missing any labs. If you miss a lab, it is your responsibility to obtain assignments and other information given on that day. You will not be penalized for the first missed lab. However, each additional missed lab will result in loss of 5% of the overall grade up to a total of 10%.
- ◆ Common courtesy is expected in class. Please turn off your cell phone or put it on silent mode while in class.
- ◆ Please make sure you save your graded labs. I may ask for them in case of any grading discrepancy.
- ◆ "I" indicates that the student has done satisfactory work in the course, but because of circumstances beyond his control has been unable to finish all requirements. It is not to be given to enable a student to do additional work to bring up a deficient grade.

### **Campus-wide Policy Statements**

**a. Academic integrity policy statement.** See [www.newpaltz.edu/advising/policies\\_integrity.html](http://www.newpaltz.edu/advising/policies_integrity.html).

**b. Reasonable accommodation of individuals with disabilities statement.** This language is recommended: Students with documented physical, learning, psychological and other disabilities are entitled to receive reasonable accommodations. If you need classroom or testing accommodations, please contact the Disability Resource Center, Student Union Building, Room 210, 257-3020. The DRC will provide forms verifying the need for accommodation. As soon as the instructor receives the form, you will be provided with the appropriate accommodations. Students are encouraged to request accommodations as close to the beginning of the semester as possible.

**c. Identity verification policy statement for online courses.** See [www.newpaltz.edu/advising/policies\\_onlineverification.html](http://www.newpaltz.edu/advising/policies_onlineverification.html).

Also note Computer Services' acceptable-uses policy (<http://csc.newpaltz.edu/policies/acceptable-uses-and-privacy-policy/>), which states: Use of the computer resources and network facilities generally requires that you have a valid user account. You are responsible for the safeguarding of your computer account. Your account and network connection are for your individual use. A computer account is to be used only by the person to whom it has been issued. You are responsible for all actions originating through your account or network connection. You must not impersonate others or misrepresent or conceal your identity in electronic messages and actions.

**L. Information on electronic SEIs, which students are encouraged to complete.** The Fall 2013 end-of-semester SEIs will be administered **December 2-10**. You are

responsible for completing the Student Evaluation of Instruction (SEI) for this course and for all your courses with an enrollment of five (5) or more students. I value your feedback and use it to improve my teaching and planning. Please complete the form during the open period on-line.

**Special dates:**

Monday September 3	No class (Labor Day)
Monday October 11	Mid-Point of Fall 2013 semester
Monday Oct 14	No Class (Columbus Day)
Tuesday Oct 14	No Class (Fall Break)
Friday November 1	Last day of the semester to withdraw without a penalty grade
November 27 – 29	No classes (Thanksgiving Break)
December 2 - 10	SEI Administration
December 4	<b>Last lab session and Presentation Day</b> Final Exam 10:15 AM – 12:15 PM