Xilinx Verilog

< Design Suite Version: 14.1>

Tutorial

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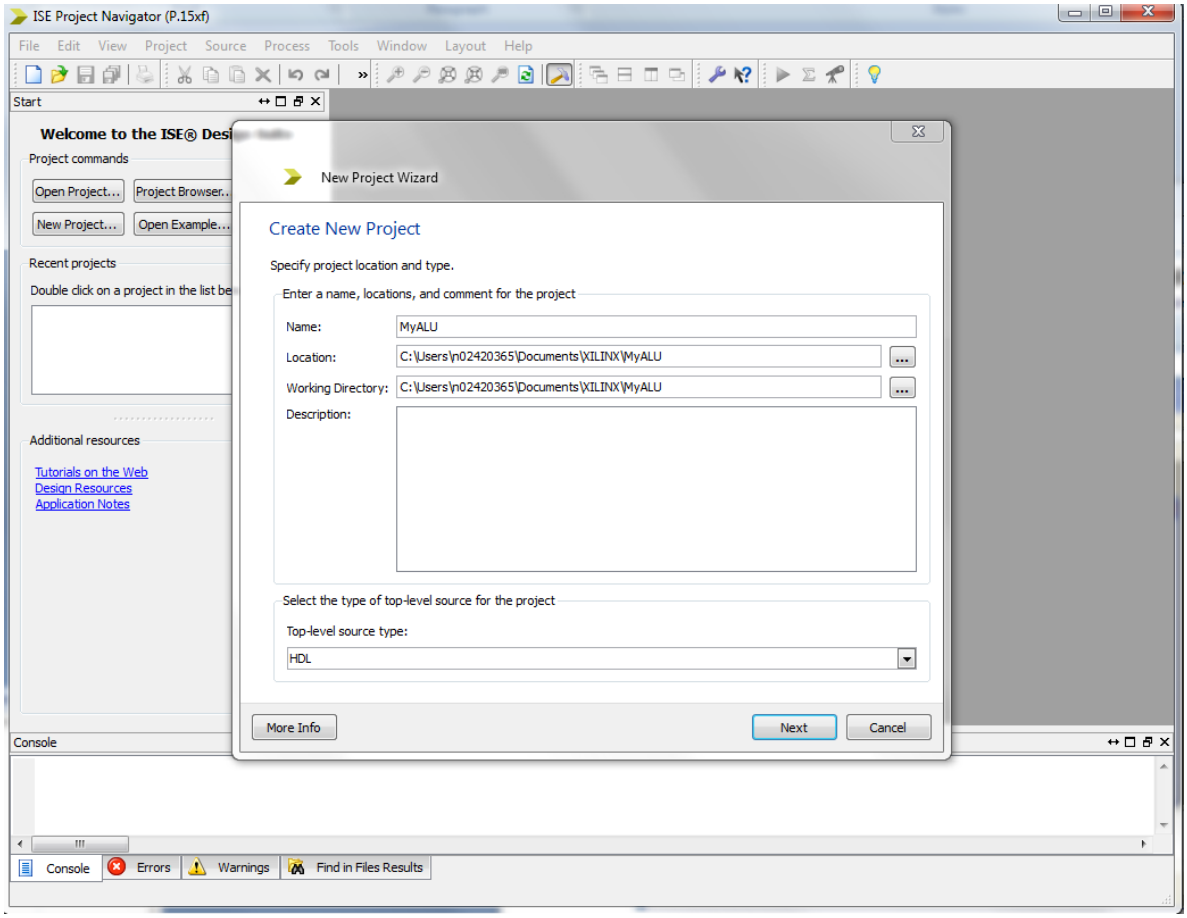
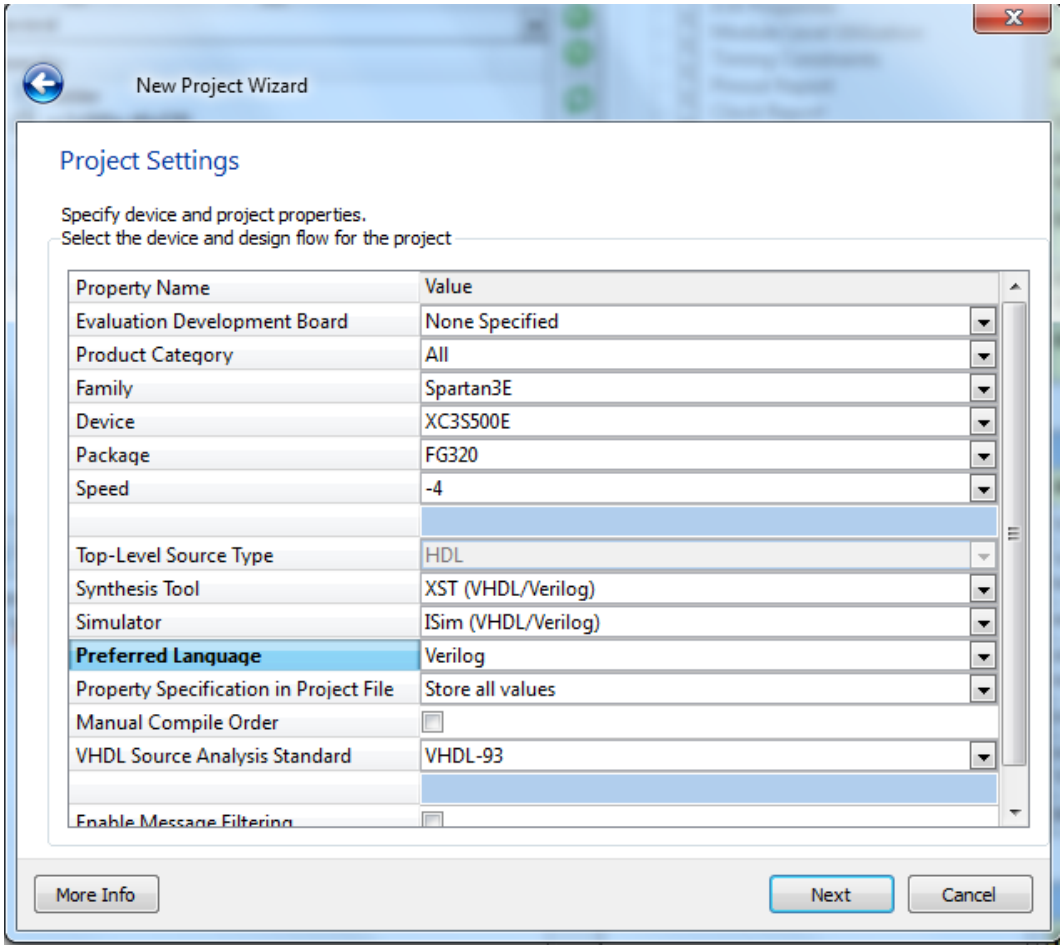
1. Start A New Project.



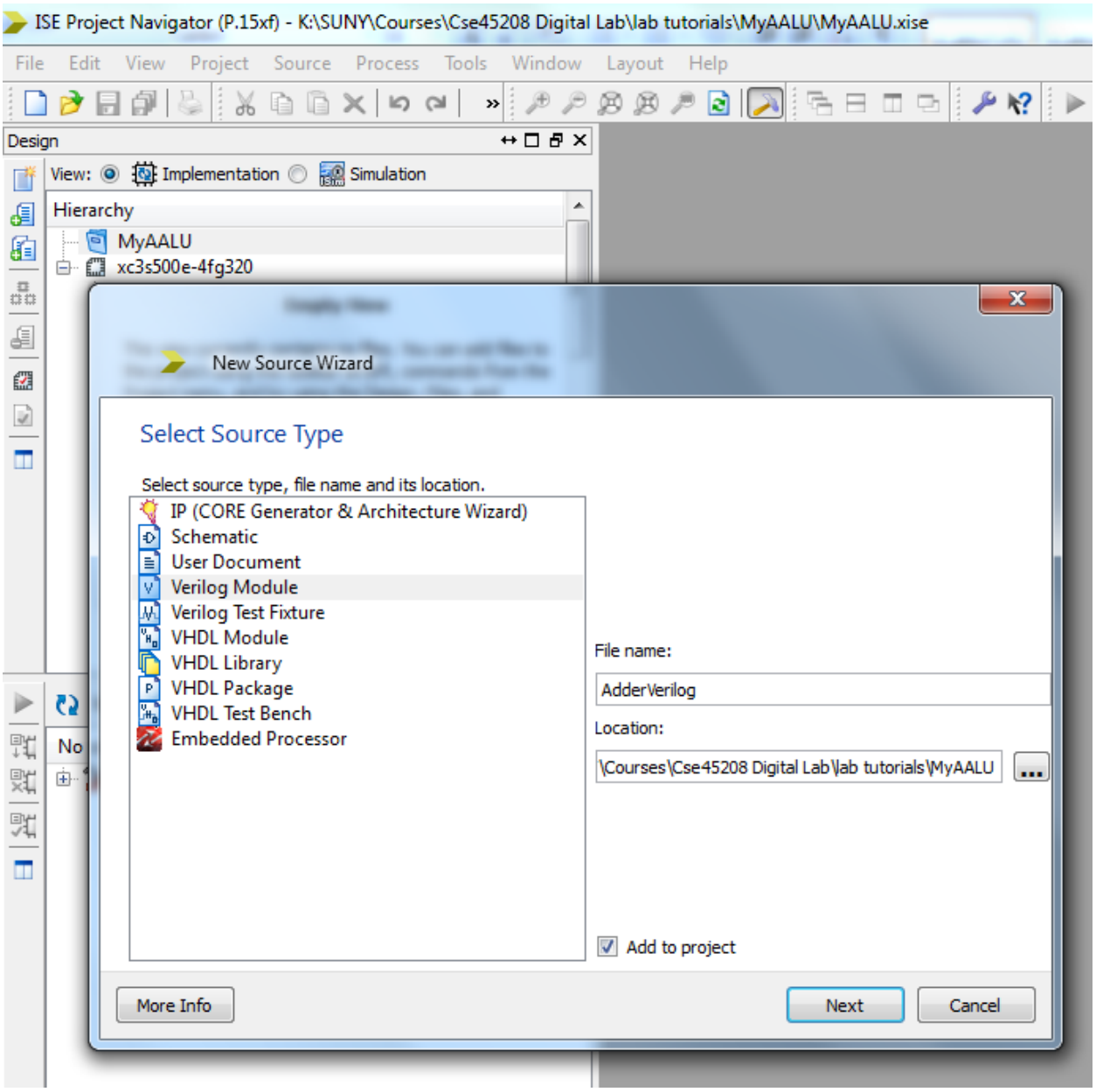
Click Next.

Make Sure the Device Properties are chosen as shown below.



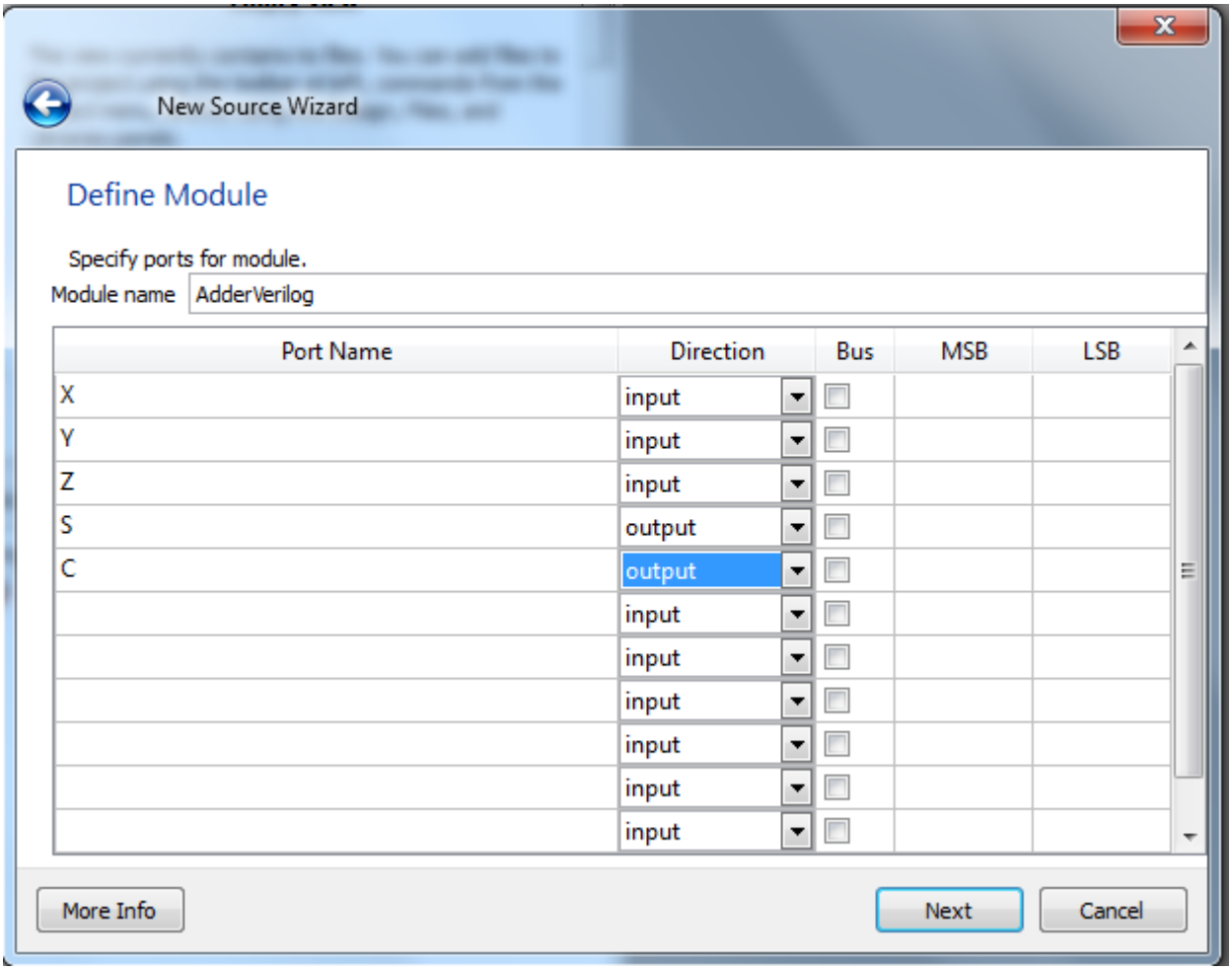
Click Next.
Click finish.

2. Go to **Project** <- **New Source**
On the New Source Wizard, click on **Verilog module** and type a filename.



Click "Next".
Click "Finish".

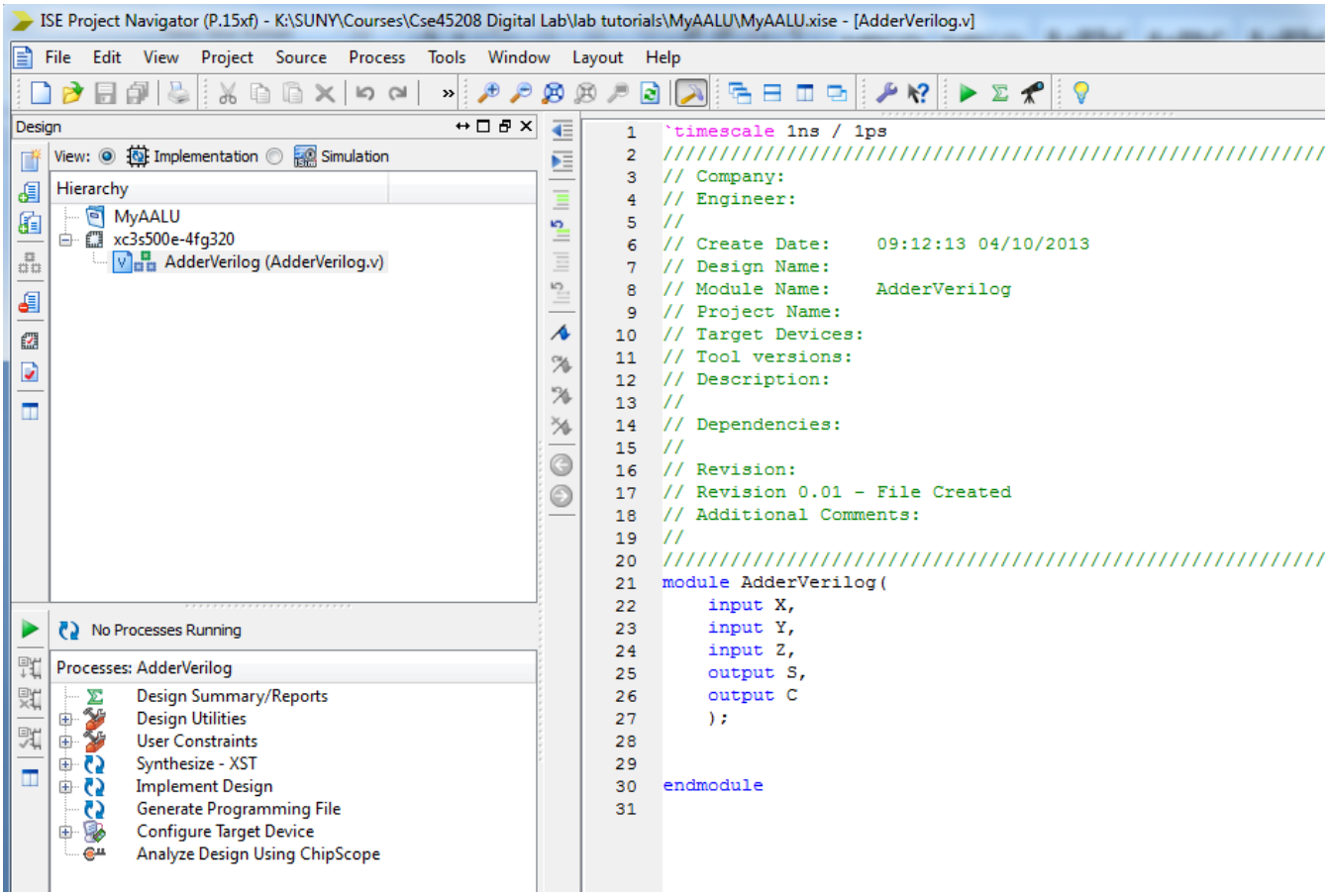
3. In this exercise, you are designing a full adder with X, Y, and Z as inputs and S and C as outputs. Hence, set the ports accordingly.



Click "**Next**"

Click "**Finish**"

4. This will open the editor where you can input your VHDL code.



Note that

$S = X \oplus Y \oplus Z$
$C = XY + YZ + XZ$

Hence, you may add appropriate equations to the module. Note the following operators

&	and
~&	nand
|	or
~|	nor
^	xor
^~ or ~^	xnor

S = X^Y^Z

C= (X&Y) | (Y&Z) | (X&Z)

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date:    09:12:13 04/10/2013
7  // Design Name:
8  // Module Name:    AdderVerilog
9  // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21 module AdderVerilog(
22     input X,
23     input Y,
24     input Z,
25     output S,
26     output C
27     );
28 assign S = X^Y^Z;
29 assign C= (X&Y) | (Y&Z) | (X&Z);
30
31
32 endmodule
33
```

5. Save the file.

The project can be simulated using ISIM simulator as described in its tutorial

When the design is completed, open the User Constraints Editor and assign the pins to the correct inputs and outputs. Follow the steps in the Download Tutorial to complete the process.