State Diagram Tutorial

written by
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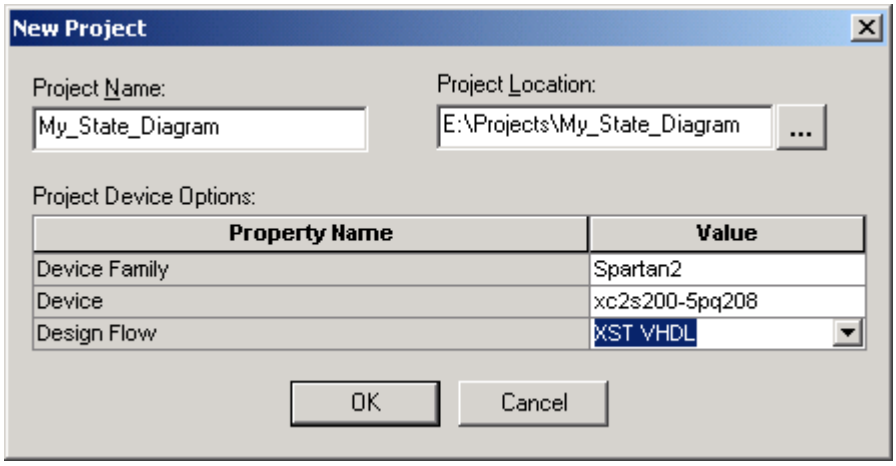
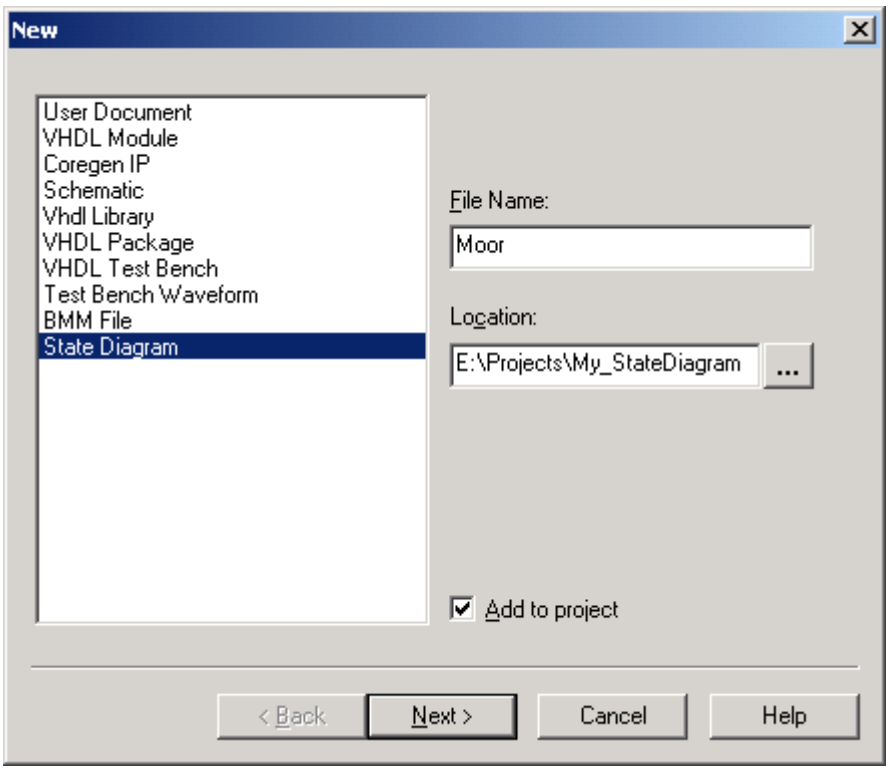
10/29/02

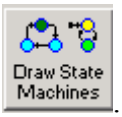
Start a new Project and Select the correct chip setup for the Digilab 2 boards.



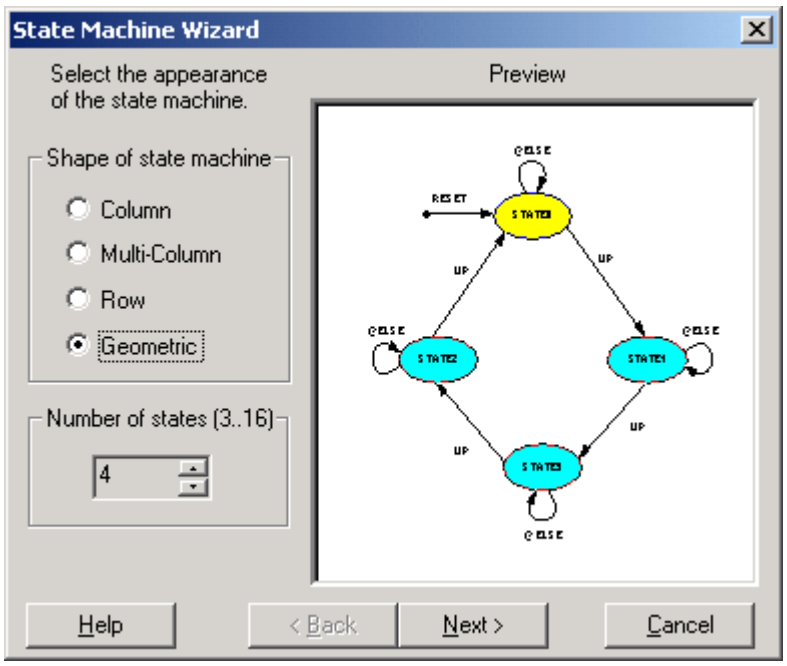
Hit OK. Then right click on the device and select New Source…



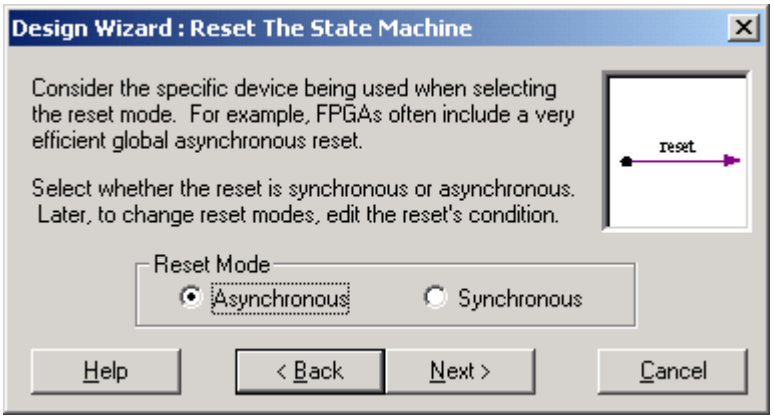
Select State Diagram and give the file a name. The File name needs to be 8 or less characters. Then Hit Next. Then Finished. This will open up StateCAD.

Once StateCAD is open click on the button Drawn State Machine 

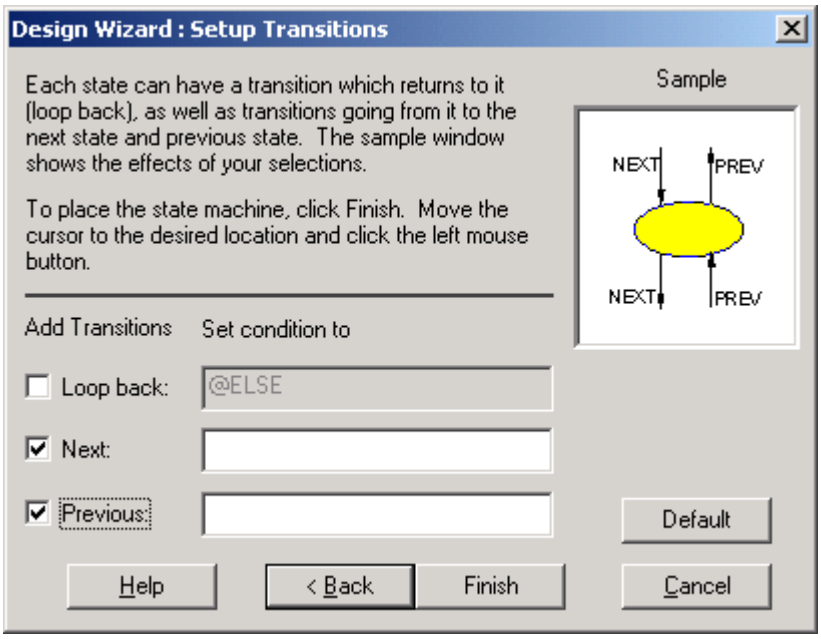
. This will open a State Machine Wizard that will guide you through the process of creating a State Diagram. Select a geometric diagram with 4 states and then click "Next.



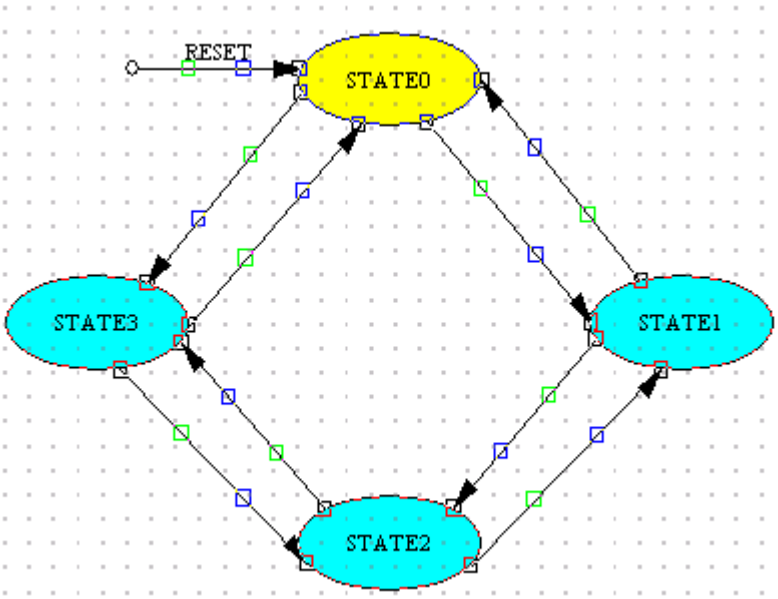
Select an Asynchronous Reset, then hit “Next”.



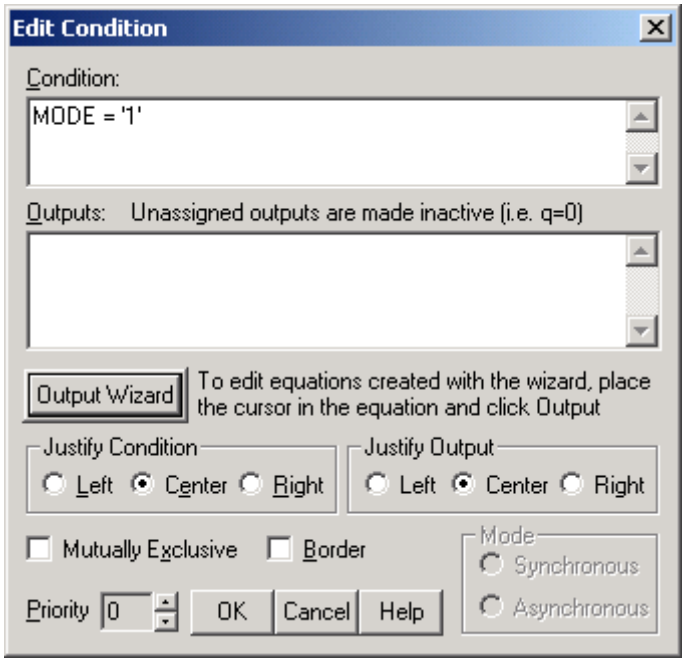
To setup the transitions from one state to another, select both the "Next" and "Previous" options in the "Setup Transitions" window. Click on "Finish" to create the state diagram.



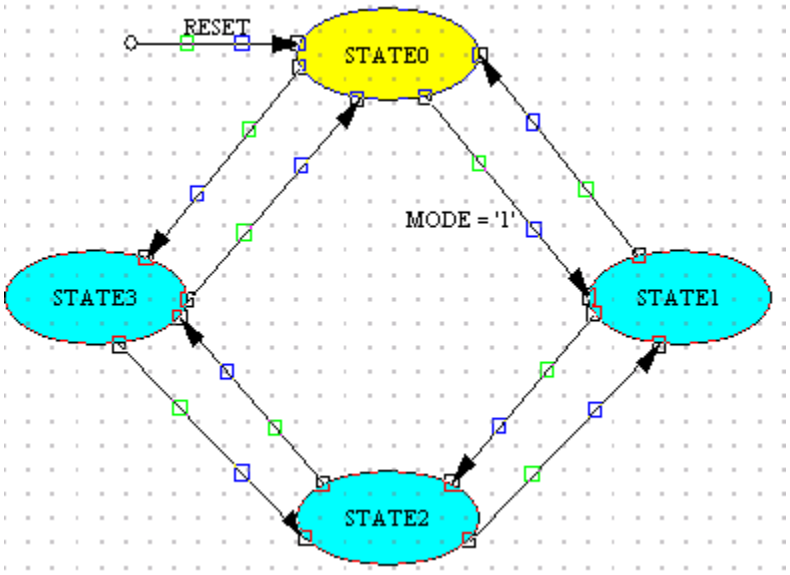
Now that the template state diagram has been created, it still needs to be placed onto the blank diagram window. To place the diagram created from the wizard, left-click anywhere on the blank diagram; an inch from the top-left corner is a good place.



Now that the basic diagram is in place, we need to add/remove/modify the current transitions to obtain the correct state diagram for the sequence generator. Left-click on one of the two boxes of the transition arrow **State0-->State1**. This will bring up the "Edit Conditions" dialog box. Add the condition **MODE = '1'** in the "Conditions" box.

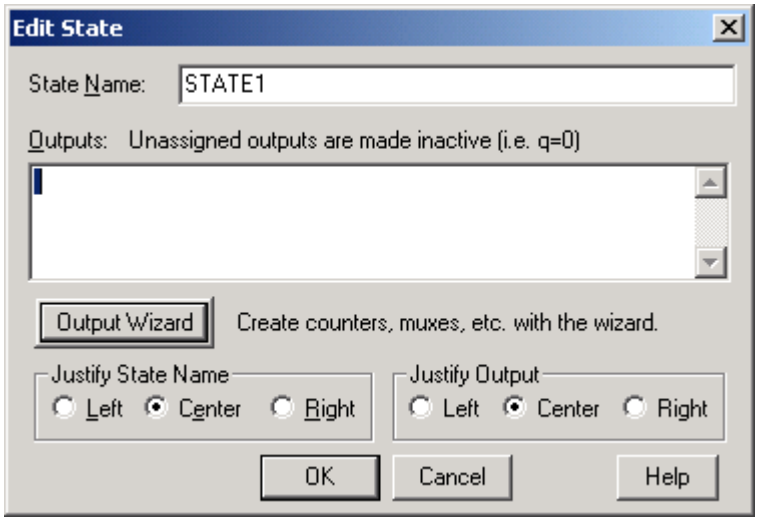


This condition will make the transition **State0-->State1** occurs when **MODE** is true or '1'. Click "OK". Your diagram will now have the condition on the transition line.

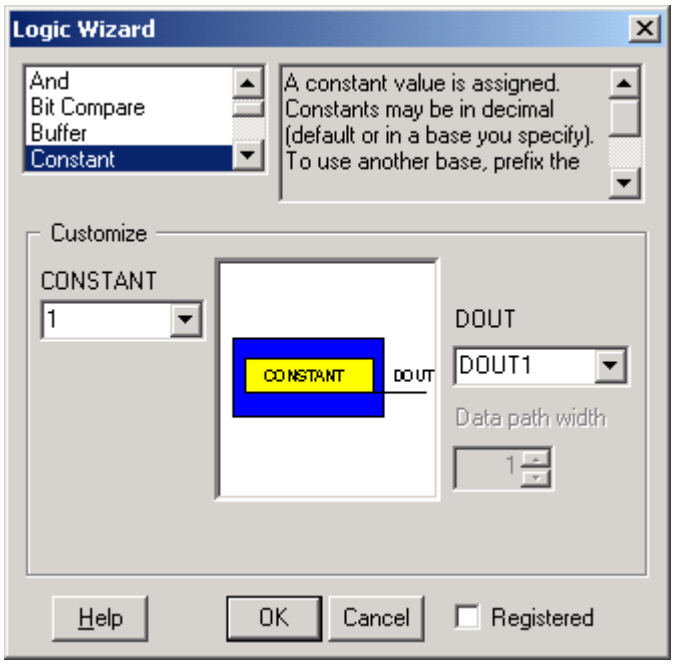


At some point you will need to resize and move the transition text so as to make it more readable and organized. This can be done by holding down the left mouse button and moving the mouse accordingly.

Double click on State1.

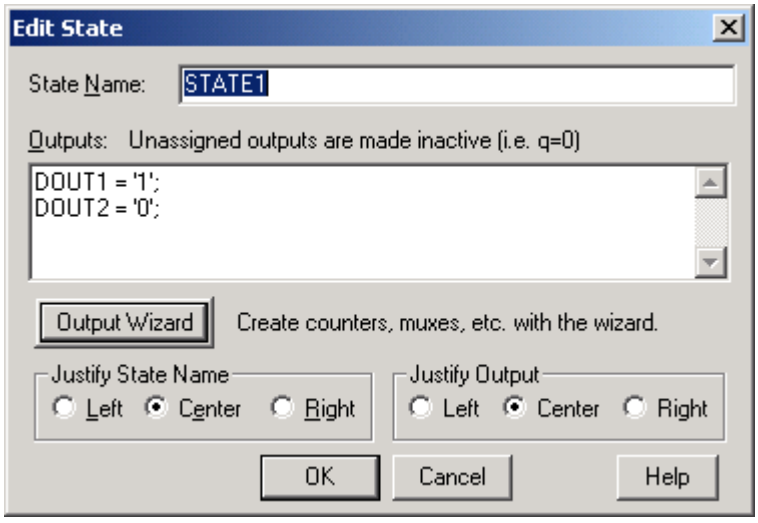


To assign the correct output for that state, click on the "Output Wizard" button. Select "Constant" from the upper left box, type 1 in the "CONSTANT" box, type DOUT in the "DOUT1" box, and set the "Data path width" to 1. Click on "OK".

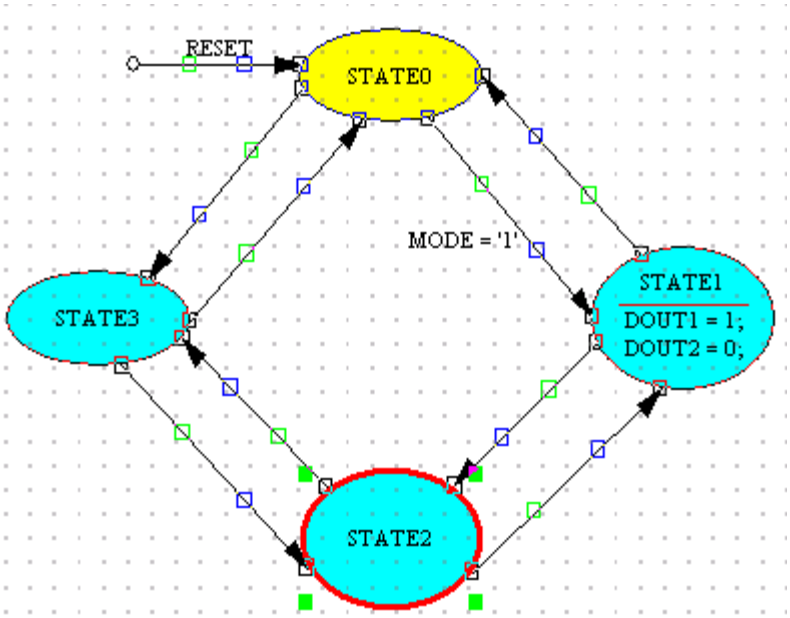


Do this process again but this time define an output “DOUT2” with data width 1. Click “OK”.

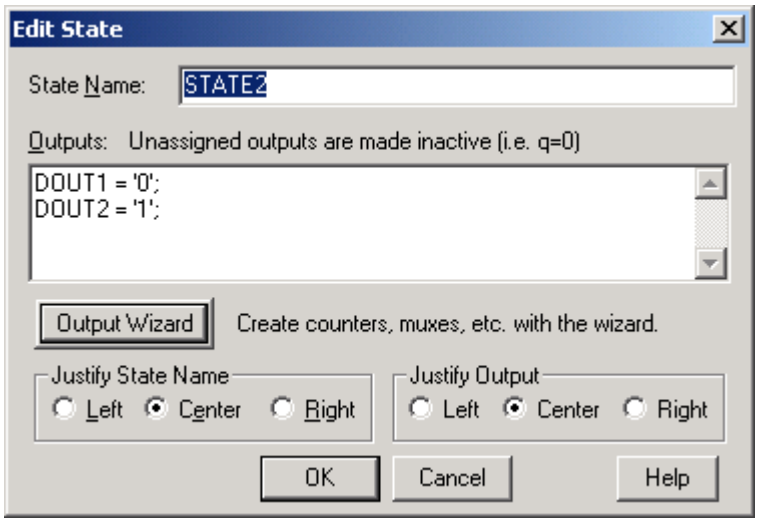
Now your state has defined outputs.

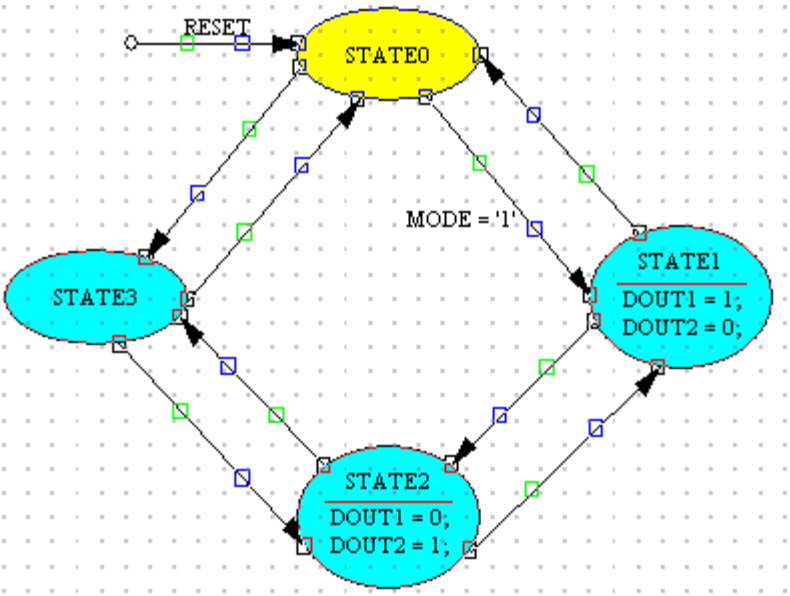


Click “OK”. You can see the outputs of State1 on the diagram.

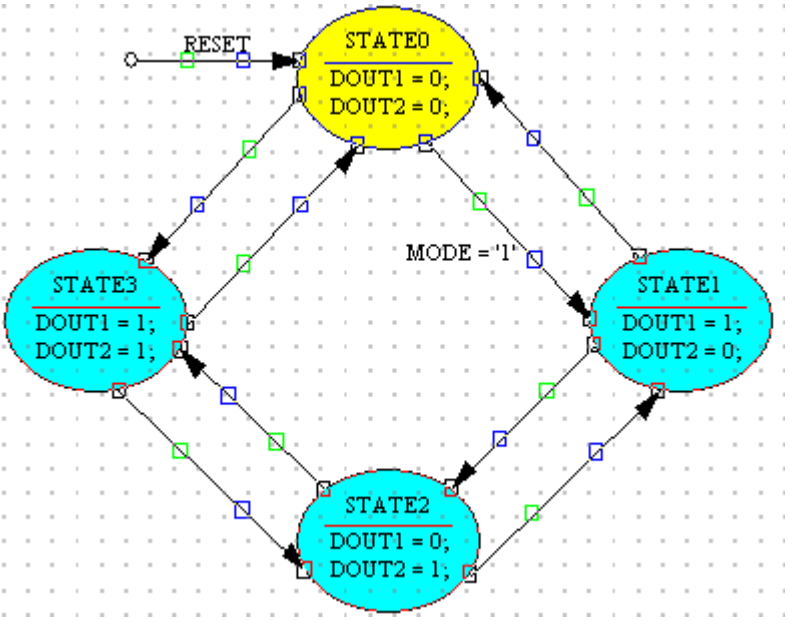


Now that the two states have been defined we do not need to run the “Output Wizard” again. Now double click State2. Edit the outputs as seen below. Click “OK” when done.





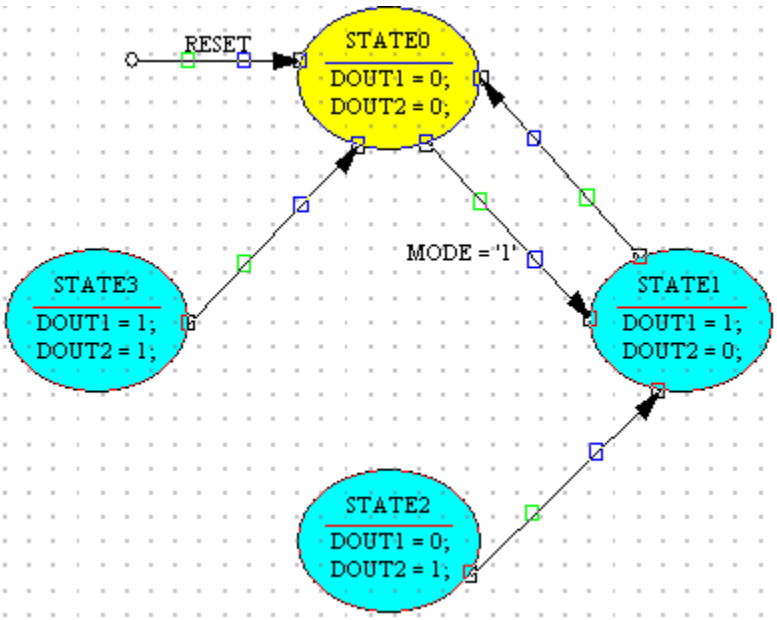
Continue till all States have outputs as defined below.



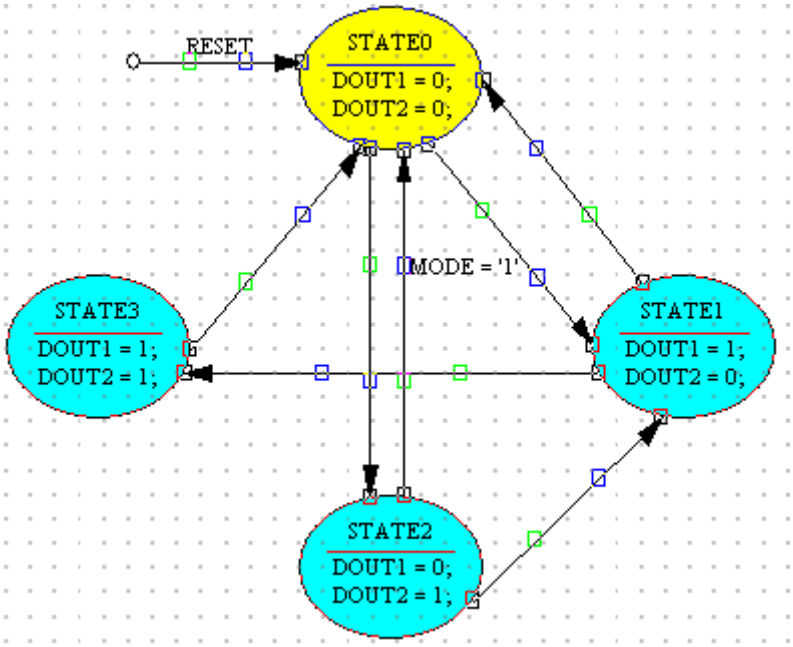
Since not all of the transitions from the template are needed, they need to be deleted by left clicking on the transition line and pressing the delete key. The following state transitions need to be deleted:

State0-->State3
State2-->State1
State2-->State3
State3-->State2

The state diagram should now look like this:



We now need to draw the state transitions **State0-->State2, State1-->State3, State2-->State0**. To do this, press the button with the blue curved line  on the left toolbar. Left-click on the edge of **State0** to start the beginning of the transition, indicated by a red box, and once more at the edge State2 to end the transition. Do the same from **State1** to **State3** and **State2** to **State0**. The state diagram should now look like this.



Finish the diagram by applying the following conditions and outputs for each transition:

State0-->State2
Condition: MODE = '0'

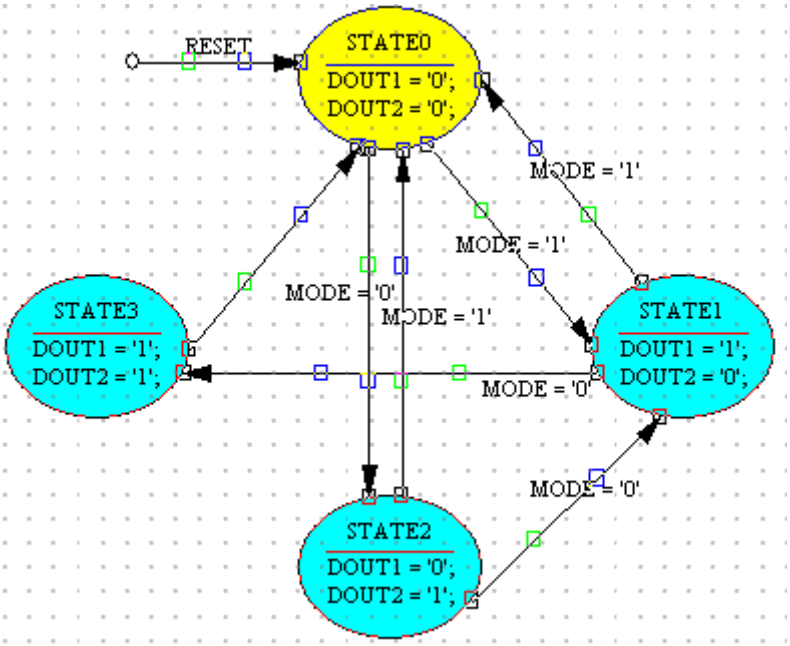
State1-->State3
Condition: MODE = '0'

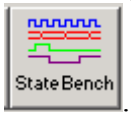
State 2-->State0
Condition: MODE = '1'

State1-->State0
Condition: MODE = '1'

State2-->State1
Condition: MODE = '0'

The final state diagram is shown below.



Now save the diagram. Now we need to test our design. Left Click on the State Bench Button 

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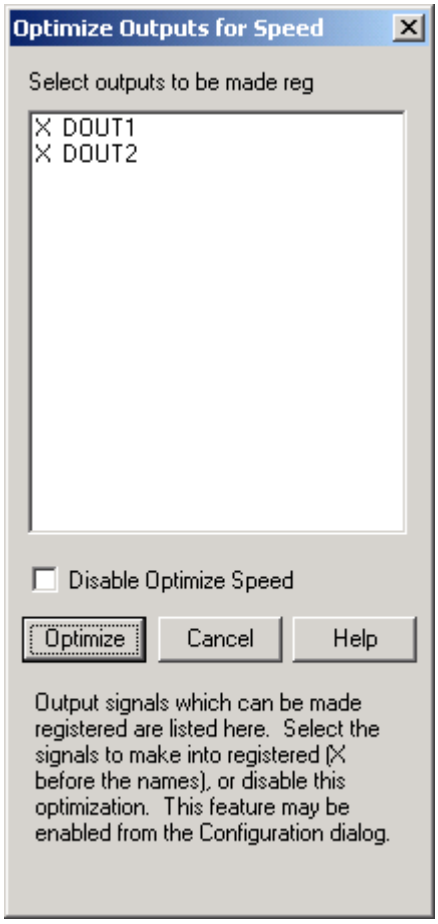
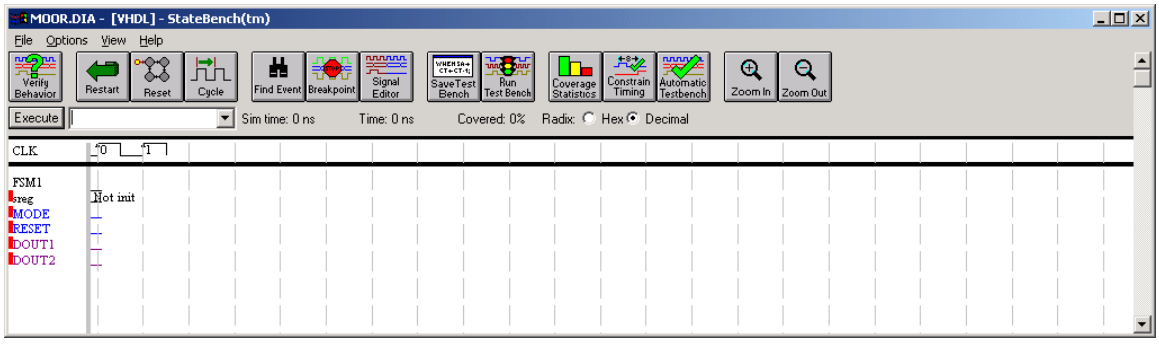
If all goes well, this dialog window will appear.

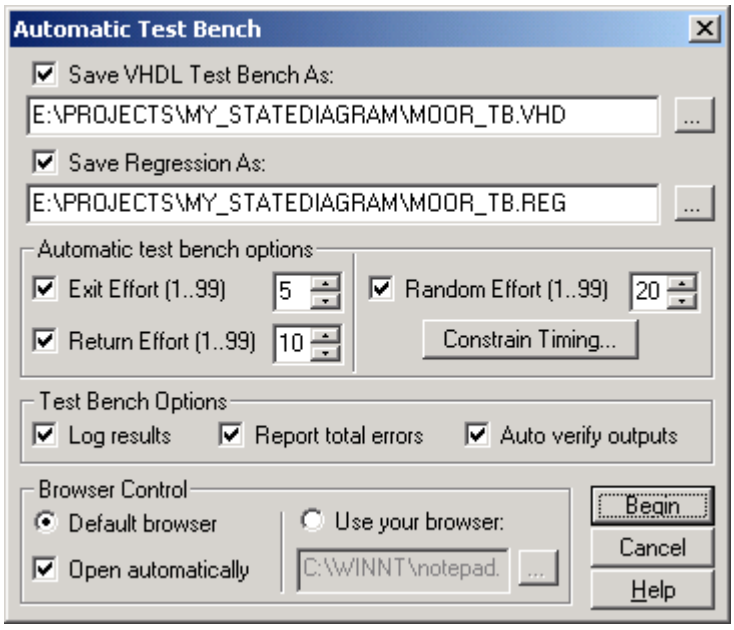


We do not want to optimize any outputs so just click “CANCEL”. Then a small waveform generator will appear after the VHDL has been compiled.

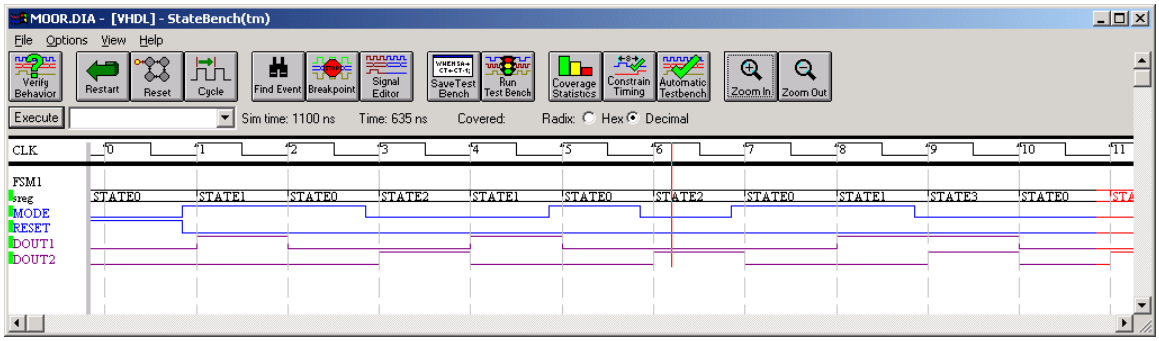


Xilinx can automatically generate every single test case possible, just by clicking this button 

. And the following window will appear.



Just click “BEGIN”. This will show you the VHDL code along with the waveform.



Verify that your design is correct by viewing the generated waveform.