ModelSim Tutorial

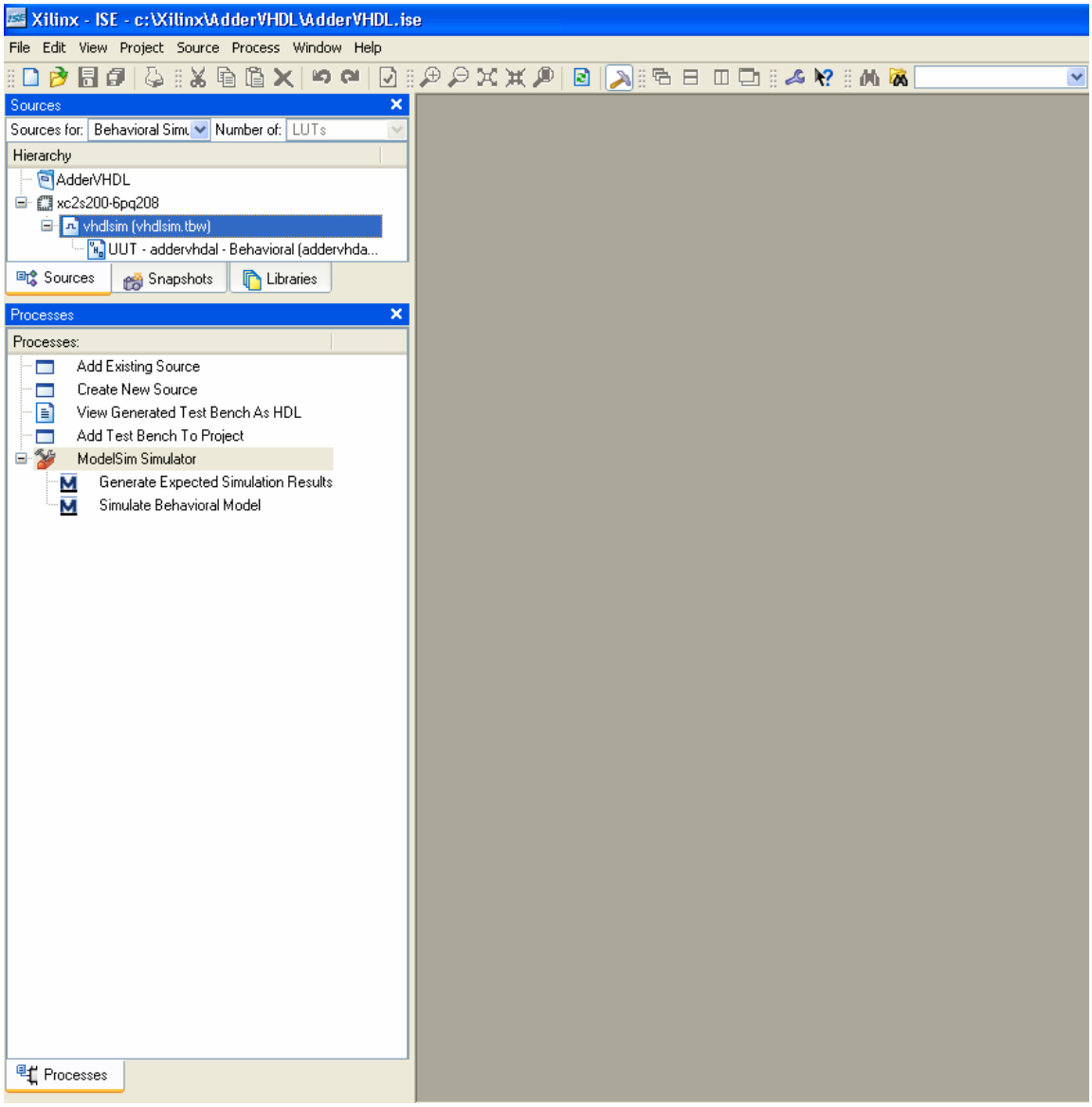
For

Xilinx

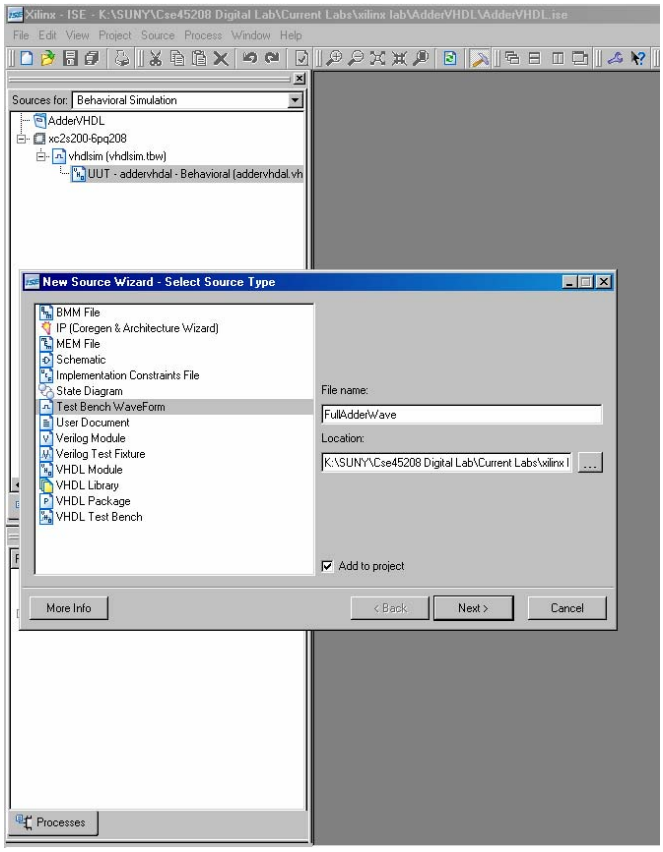
<Release Version: 8.2i>

You will next test the full adder circuit that you built in the VHDL tutorial via the ModelSIM simulation tool so that you can be sure that it functions per specification. Recall that the full adder has three inputs (X, Y, Z) and two outputs (S, C). If you have not yet saved your VHDL file yet, do so and close the Editor.

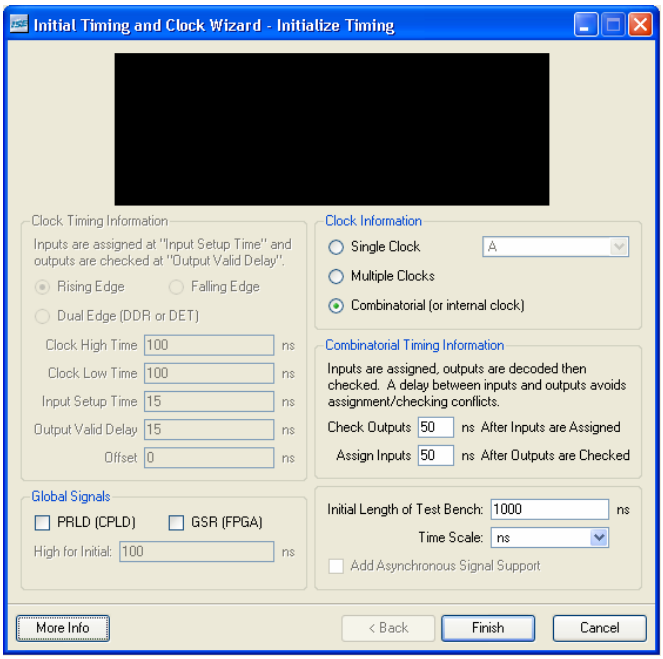
Next, go back to the Project Navigator and select Behavior Simulation for Sources. Next, highlight the source that you want to simulate. In this case we want to simulate the circuit named myfulladder. Under Processes, double click on Create New Source.



This will open a dialog box. Select “Test Bench Waveform” as the type of design entry and pick a name for your file.

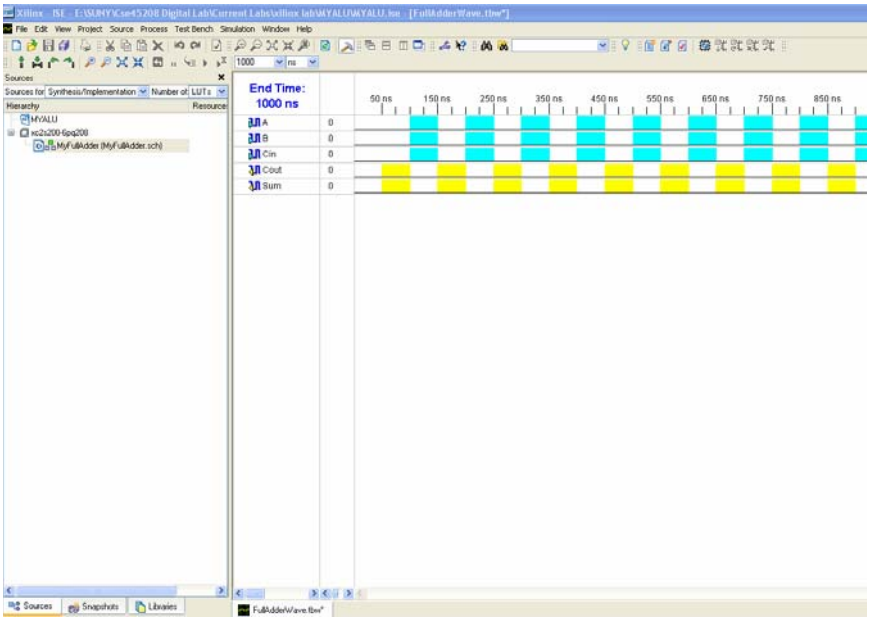


Click Next!, Next! Then Finish! This will open up the following window:

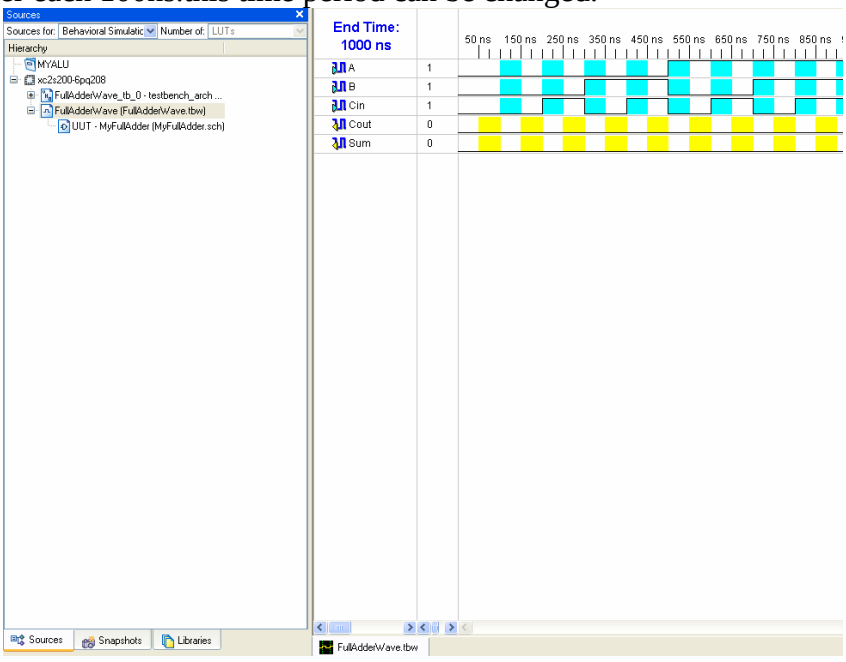


You may change the time period of your input clock cycle, among other things. Here, the circuit is combinational. Make changes and Click Finish!!!!

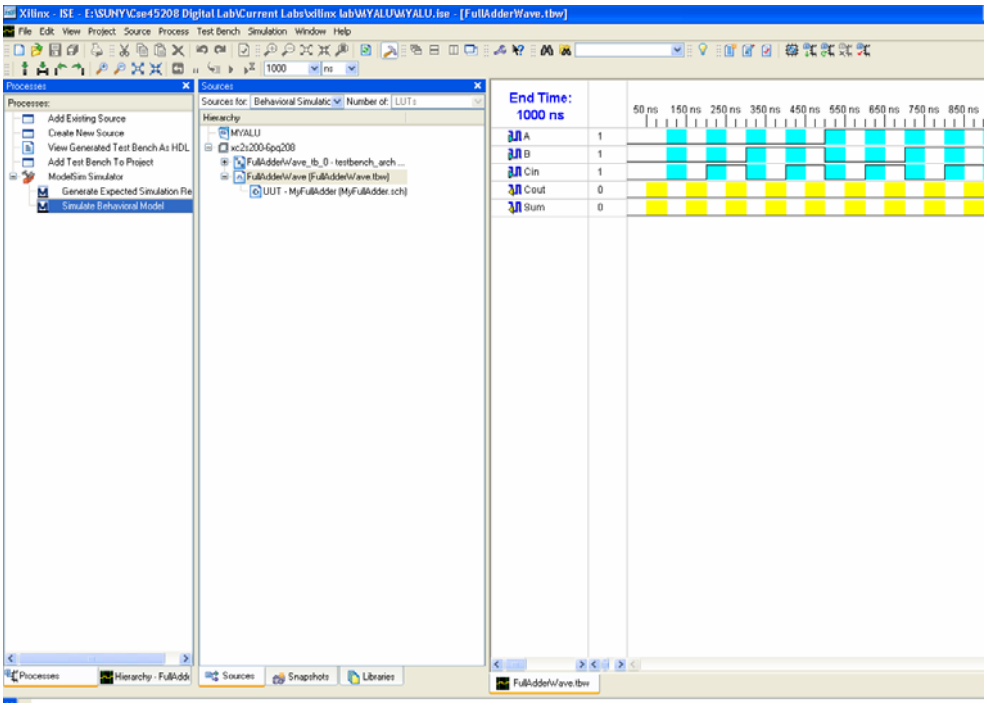
This opens the waveform window where you can select various values for the three inputs of your full adder. The input ports are marked by the blue color and the outputs by yellow.



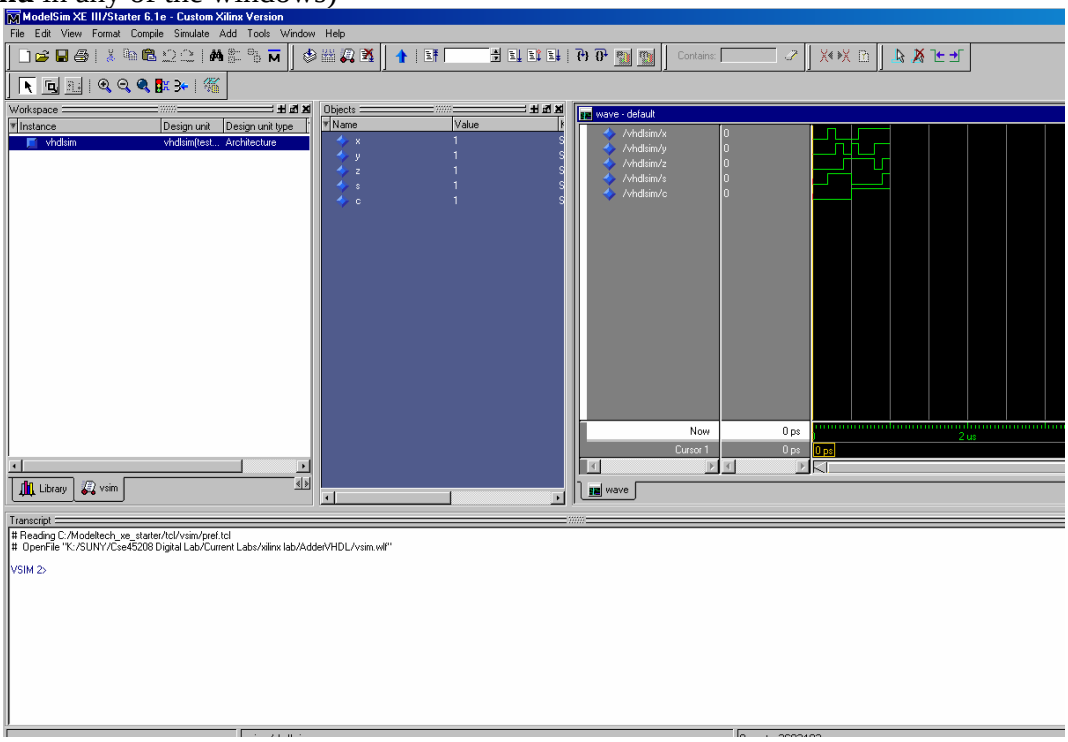
Various values (0 or 1) can be assigned to the inputs by just clicking on the blue bar corresponding to each input. Put combinations 000 through 111. The assigned values of various inputs are shown below as a waveform. A different value of input is assigned to the ports after each 100ns.this time period can be changed.



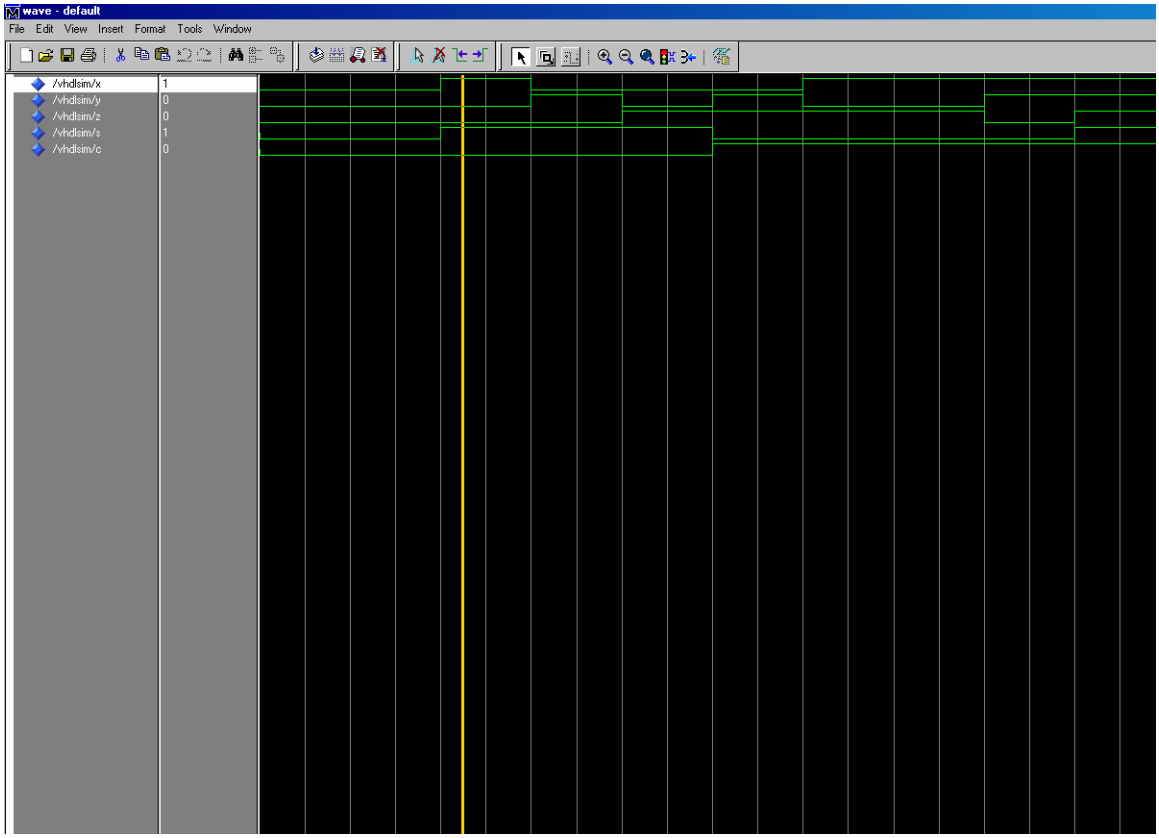
Now save the waveform. In the Processes windows, under ModelSim Simulator, Double Click on the “Simulate Behavioral Model ”.



Minimize the project navigator. The ModelSIM tool should occupy four separate windows. And look something like this. (Layout styles can be changed from the **windows menu** in any of the windows)



In the Wave window select from the toolbar, Zoom -> Zoom Full.



Take a look at the Wave window. In this window you are able to see the waveforms of your simulated design.