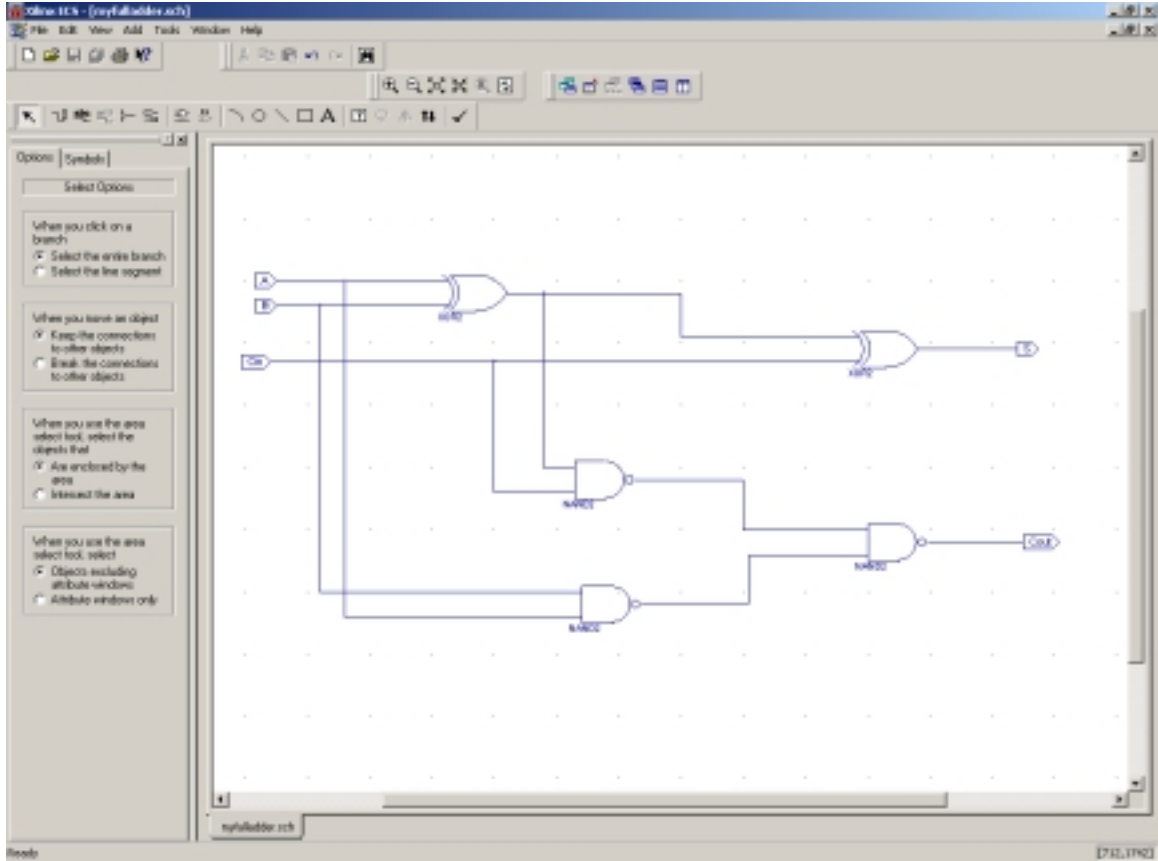


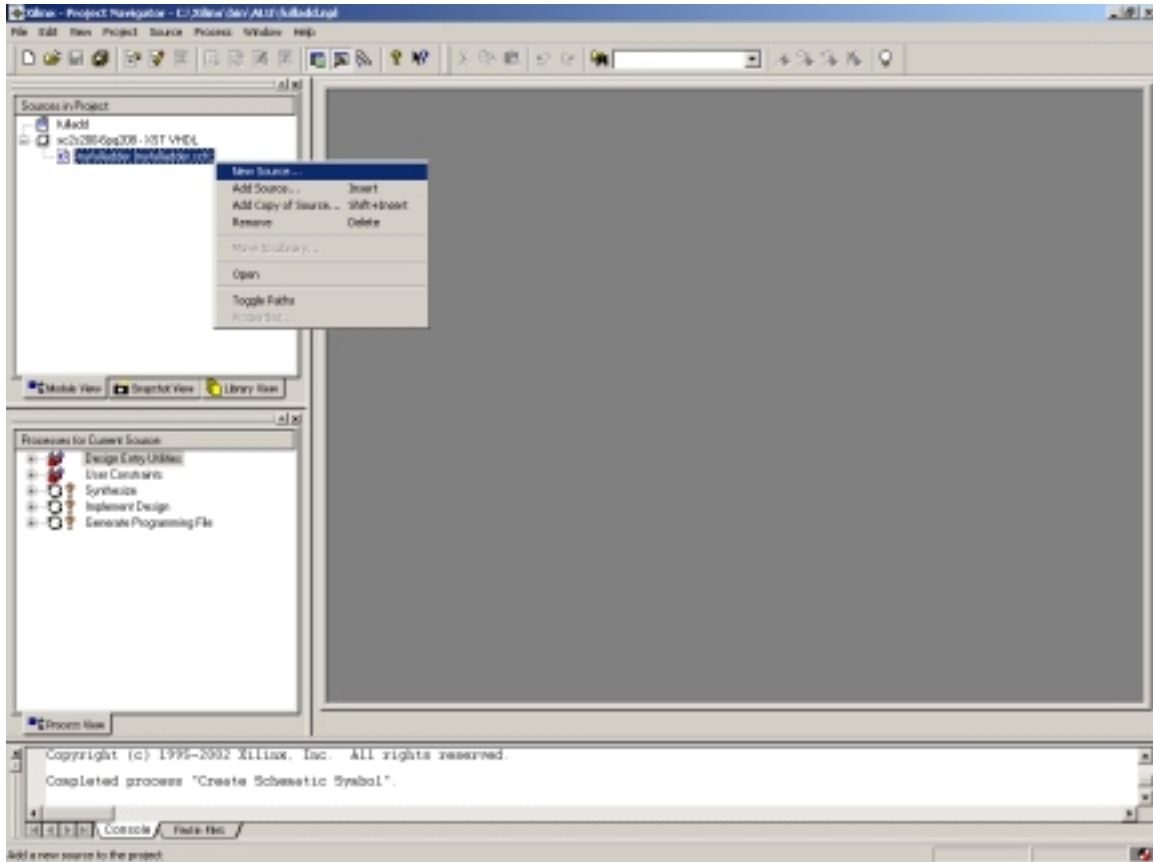
ModelSIM Tutorial

Now that you built a full adder in the last tutorial, let's make sure that it works. The way we will be testing our circuit is by using the ModelSIM (or VSIM) tool. Now let's look at our full adder.

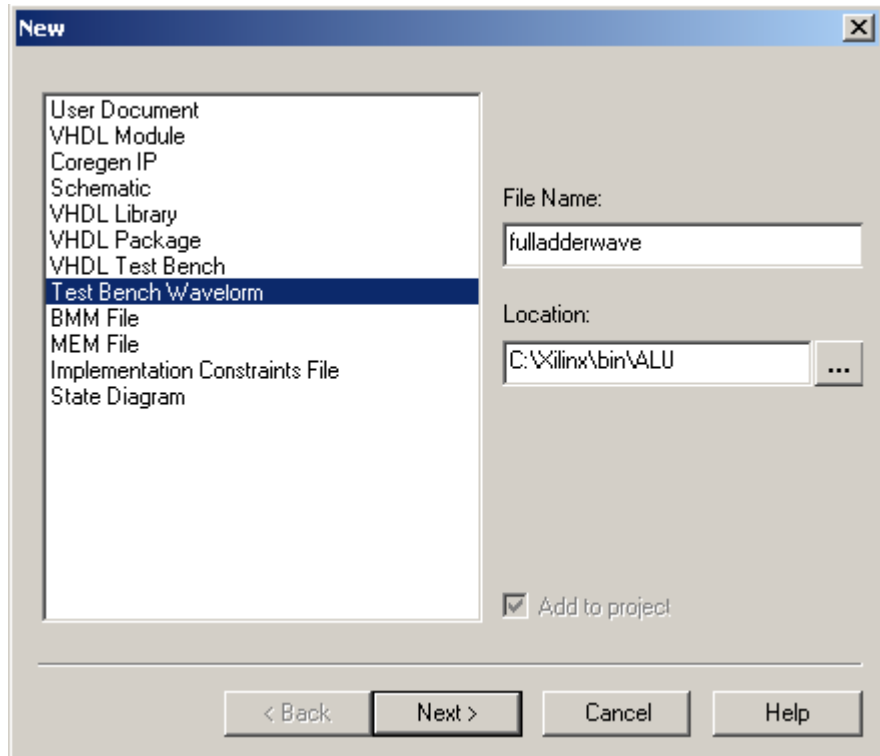


The full adder as three inputs (A, B, Cin) and two outputs (S, Cout). Now save your schematic and close the Schematic Editor.

Now go back to the Project Navigator. Highlight the source that you want to simulate; in this case we want to simulate the circuit named myfulladder. Then right click on the source myfulladder and select New Source.

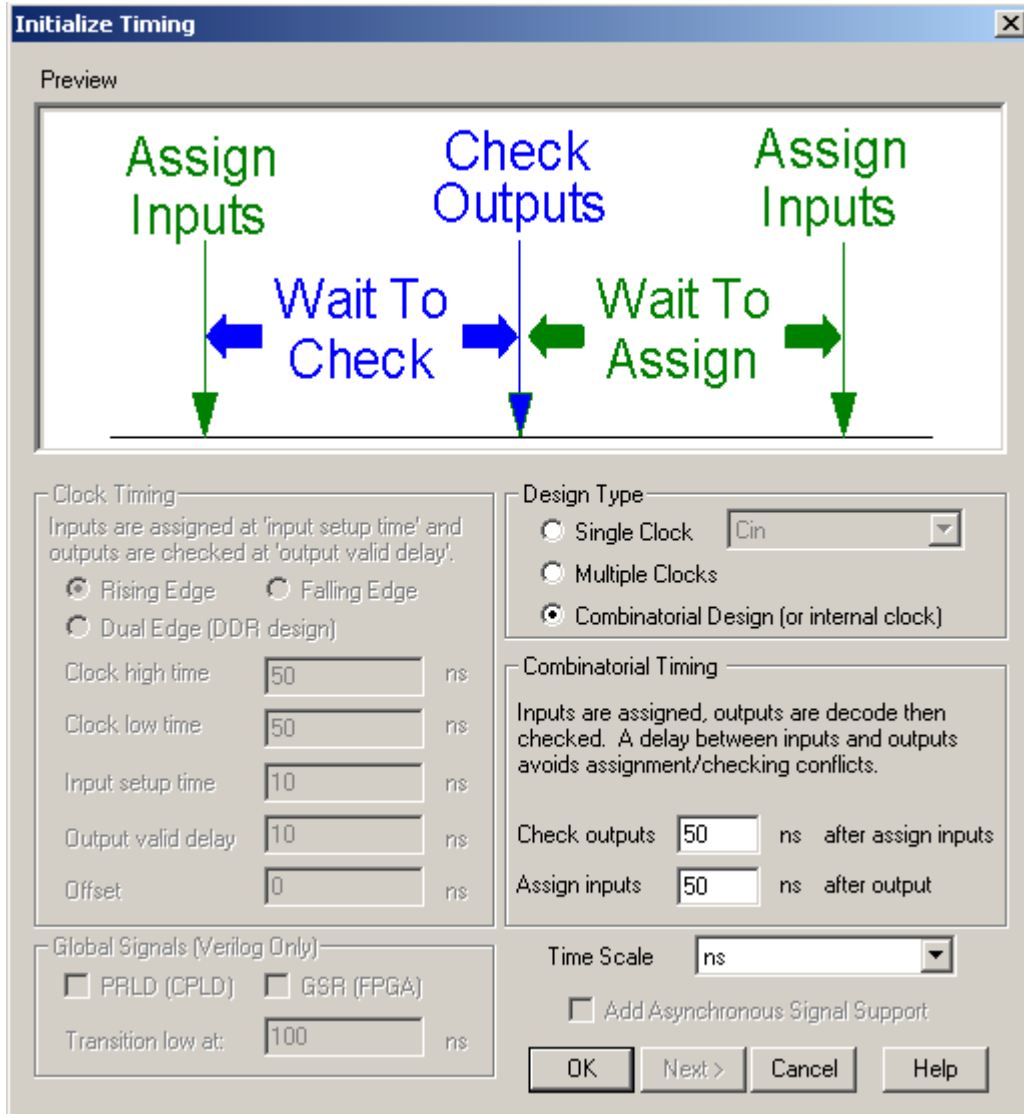


This will open a dialog box, prompting you to enter a choice for the design type and a name. Select “Test Bench Waveform” as the type of design entry. Also make sure you don’t forget to name your file.



Click Next!, Next! Then Finish!

This will open up a menu as shown below :



Here you can change the time period of your input clock cycle. After you are done Click OK!!!!

This opens the waveform window where you can select various values for the three inputs of your full adder. The input ports are marked by the blue color and the outputs by yellow. The corresponding VHDL code is shown in the bottom window.

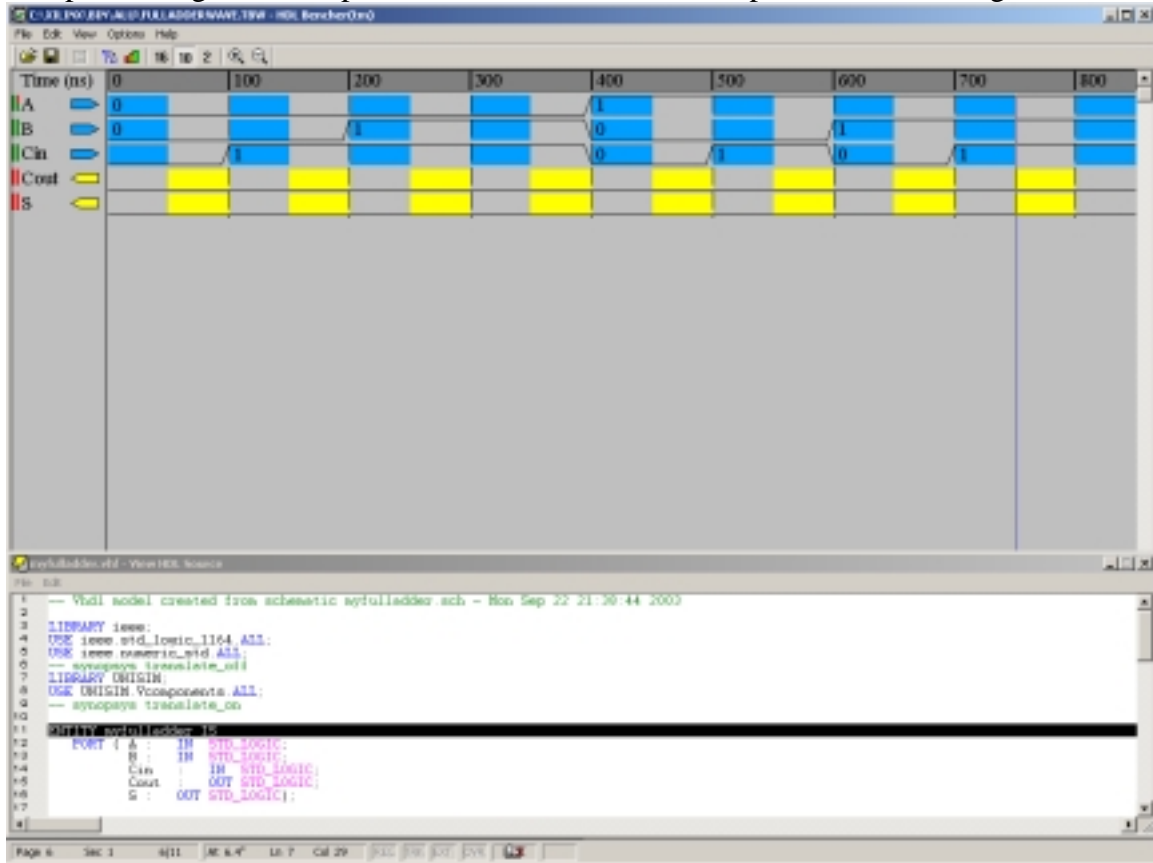
The screenshot displays a simulation environment with two windows. The top window is a waveform viewer showing the timing of signals A, B, Cin, Cout, and S over 800 ns. The bottom window shows the VHDL source code for the full adder.

Time (ns)	A	B	Cin	Cout	S
0	0	0	0	0	0
100	1	0	0	0	0
200	1	1	0	0	0
300	1	1	1	1	0
400	0	1	0	0	1
500	0	0	1	0	1
600	1	0	1	1	0
700	1	1	1	1	0
800	0	0	0	0	0

```
1 -- Vhdl model created from schematic sptfulladder.sch - Mon Sep 22 21:30:44 2003
2
3 LIBRARY ieee;
4 USE ieee.std_logic_1164.ALL;
5 USE ieee.numeric_std.ALL;
6 -- synopsis translate_on
7 LIBRARY UNISIM;
8 USE UNISIM.vcomponents.ALL;
9 -- synopsis translate_off
10
11 ENTITY sptfulladder IS
12 PORT ( A : IN STD_LOGIC;
13       B : IN STD_LOGIC;
14       Cin : IN STD_LOGIC;
15       Cout : OUT STD_LOGIC;
16       S : OUT STD_LOGIC);
17
18
```

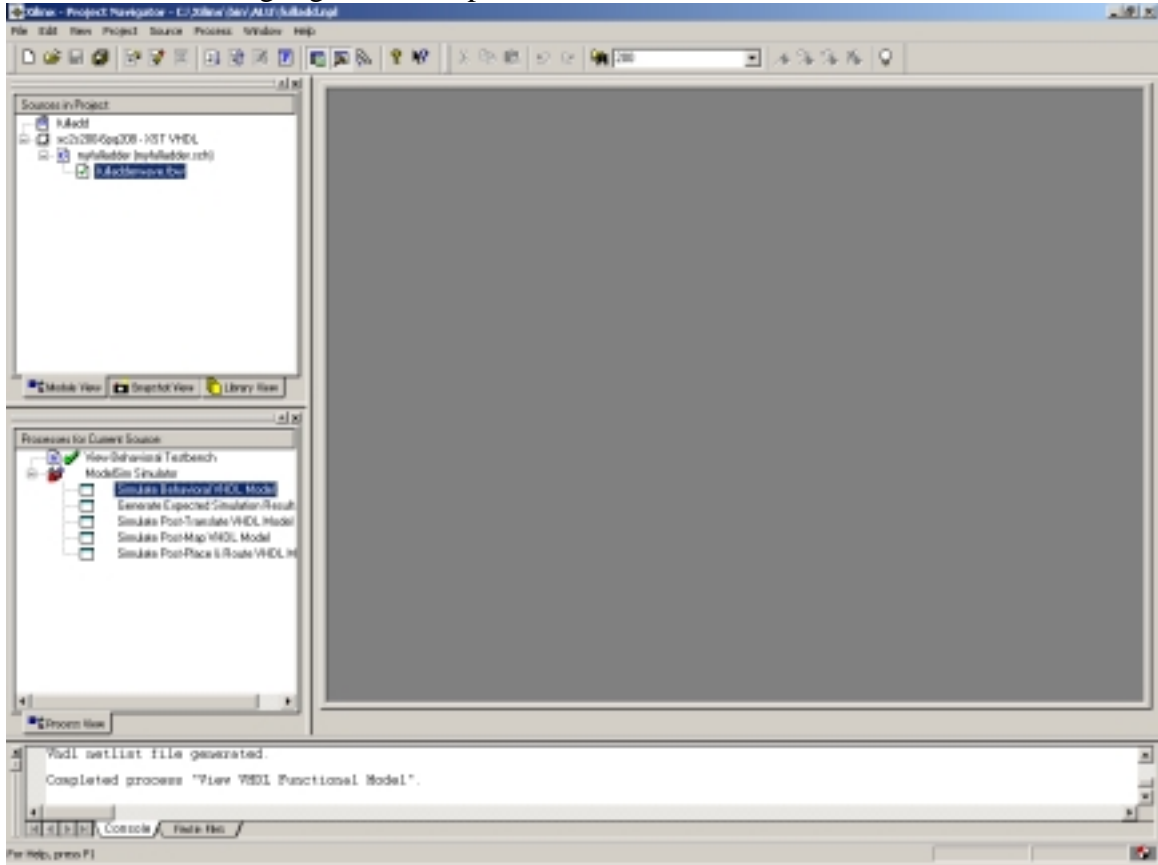
Various values (0 or 1) can be assigned to the inputs by just clicking on the blue bar corresponding to each input.

The assigned values of various inputs are shown below as a waveform. A different value of input is assigned to the ports after each 100ns. this time period can be changed.

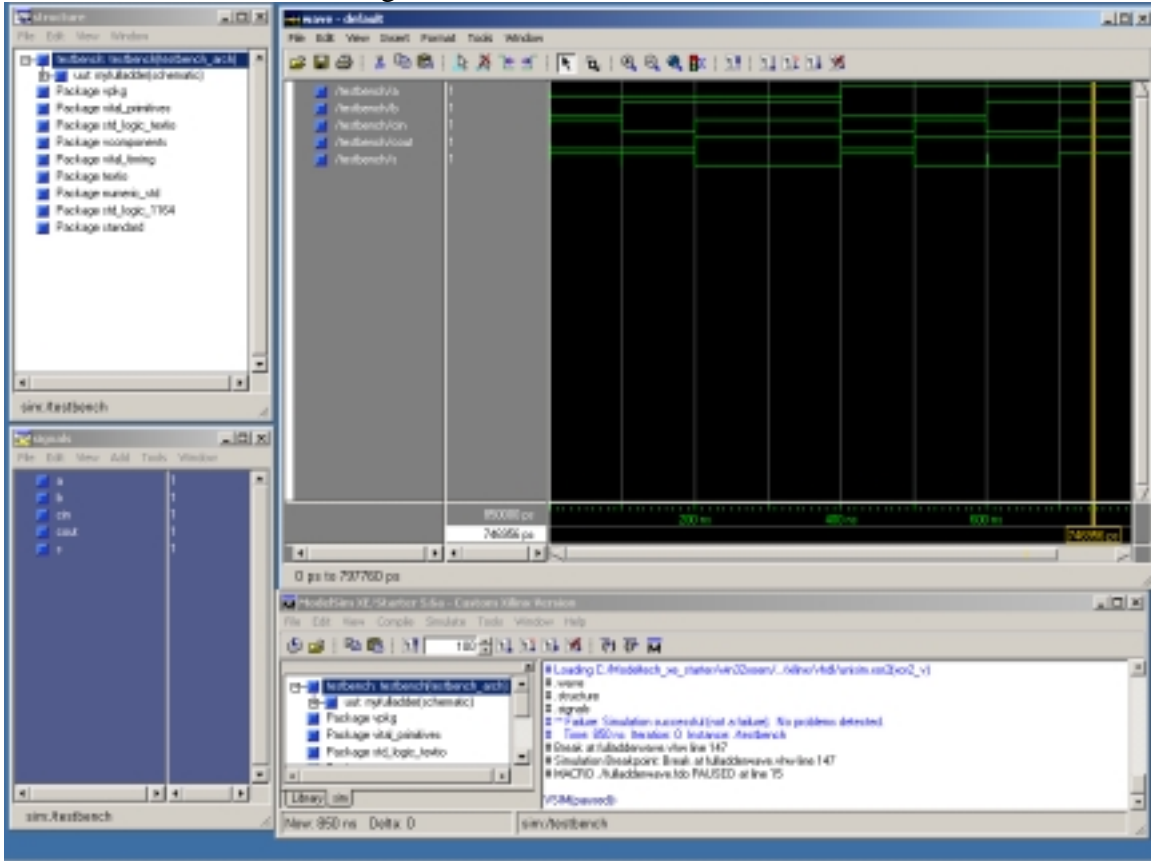


Now save the waveform, close the window and go back to the project navigator.

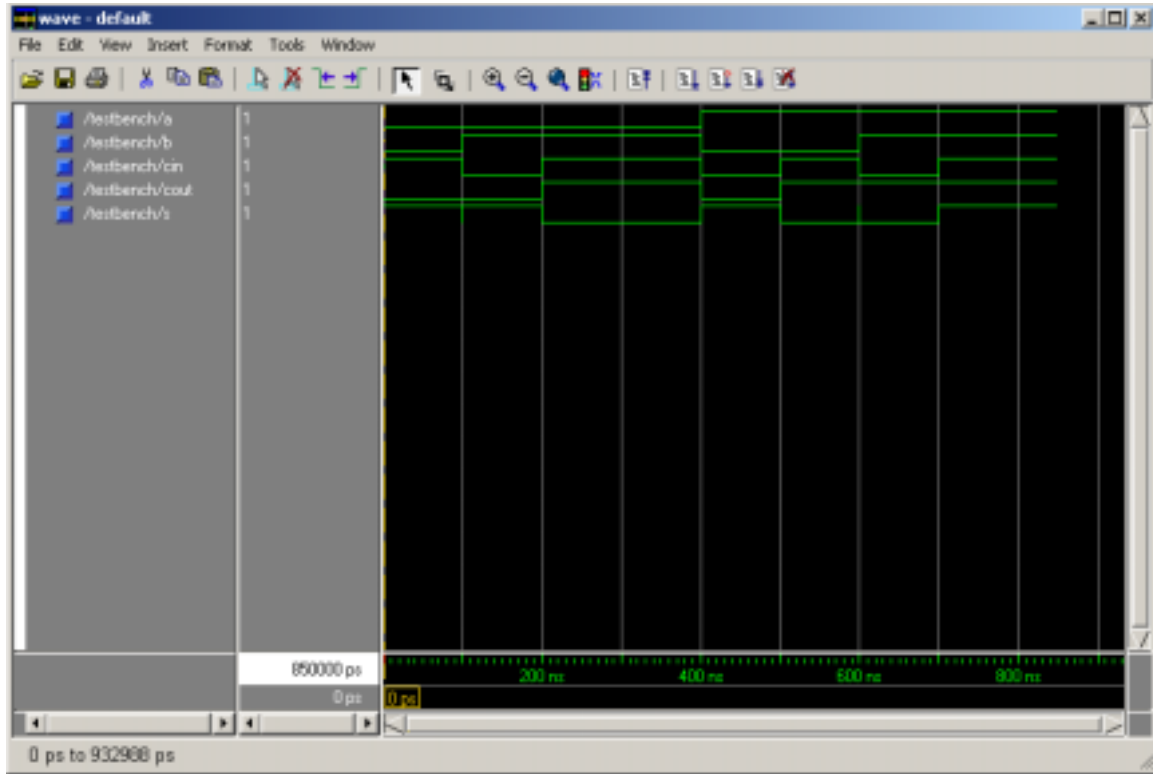
In the navigator as shown below Double Click!! On the “Simulate Behavioral VHDL Model ” which is highlighted in the processes for current source below.



Minimize the project navigator. The ModelSIM tool should occupy four separate windows. And look something like this.



In the Wave window select from the toolbar, Zoom -> Zoom Full.



Take a look at the Wave window. In this window we are able to see the waveforms of our design that we just simulated, the full adder.

Now you can do simulation for any schematic.