Lab #9 – Verilog Implementation of an Arithmetic and Logic Unit

In this lab, you are to repeat the ALU design of Lab 8 (Figure 1) using VHDL.

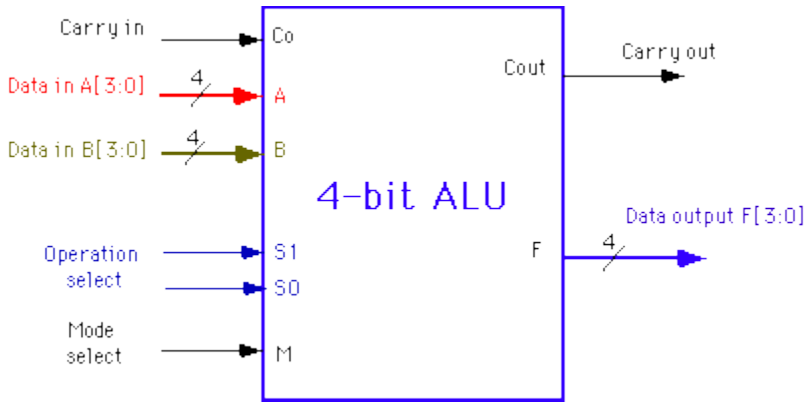

Figure 1: Block diagram of an ALU

Follow the following steps in your design process:

1. Go through the following tutorials:
   a. For a tutorial on implementing Verilog using Xilinx click Here
   b. For introduction to Verilog click Here
2. Using VDHL, design of a 4-bit ALU that performs the operations specified in Table 1. In addition, your circuit should generate N (sign), Z (zero), C (carry), O (overflow) status signals.

Table 1: Functional operation of an ALU

Arithmetic Operations:	**Logical Operations:**
Add: A + B	AND: A ^ B
Subtract: A - B	OR: A V B
Increment: A+1	XOR: A ⊕ B
Decrement: A - 1	NOT: A'

3. Simulate your design at each stage using ModelSim or ISE Simulator.
4. Download your design onto the Xilinx board.
5. Verify the circuit and have it signed by your instructor or TA.

Some suggestion to improve Xilinx performance in the lab.

1. Try to use USB flash drive
2. If you use the N drive
    a. Copy you project files to the C drive (or USB flash drive) BEFORE starting ISE/Xilinx.
    b. Start up Xilinx
    c. Load the project from the local C drive (or USB drive).
3. ***If working from the C drive***... Save frequently to the C drive but use Windows explorer to copy the project folder to the N drive. Do not use Xilinx to save directly to the N drive. This may cause a problem if, in the act of saving from within Xilinx, it changes the working environment from "C" to the network.

Reference:

1. VHDL Tutorial: Learn by Example, *Weijun Zhang*