# EGC221
# Class Notes
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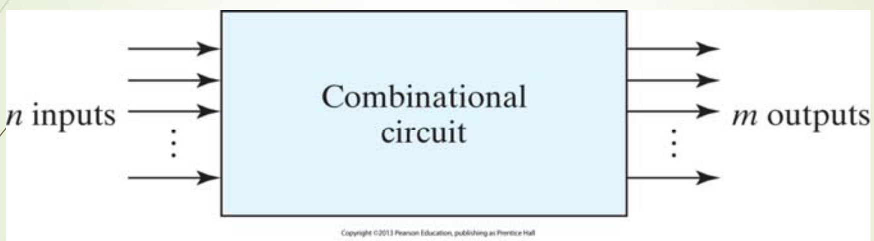
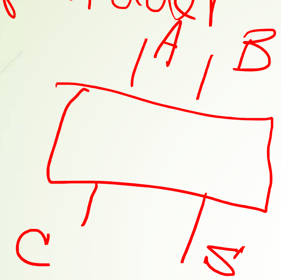
## Block diagram of combinational circuit

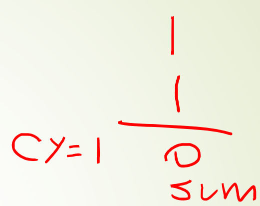


## Design Steps

- From the specification of the circuit, determine the number of inputs and outputs and assign a symbol to each.
- Derive a truth table, assigning inputs to the left and outputs to the right.
- Place all possible combination of inputs i.e all 0's to all 1's
- Using the problem definition determine each output.
- If combinations are left without a specified output, mark them as don't cares.
- Simplify each output using K-map.
- Draw a circuit for each output per requirement ie. All NAND, all NOR, AND – OR, OR – AND, XOR, etc.

## Half-Adder

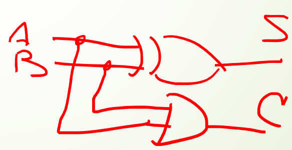


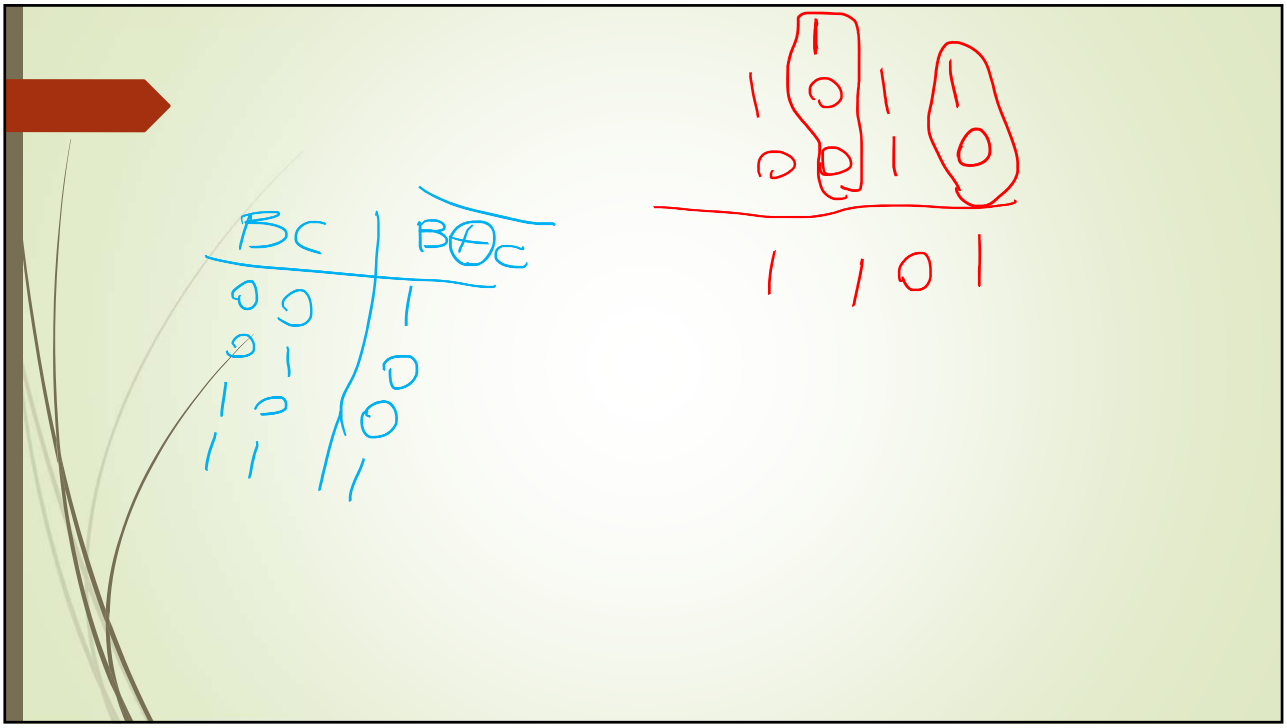




| A | B | S | C |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

$S = A \oplus B$

$C = AB$





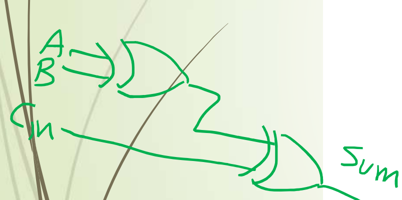

SUM = Σm(1, 2, 4, 7)
Cout = Σm(3, 5, 6, 7)

**Table 1**. 1-bit Full Adder using basic gates truth table

| A | B | Cin | **Sum** | **Cout** |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

$\overline{B}\,\overline{C} + BC = 1$

$\overline{B}\,\overline{C} + BC =$



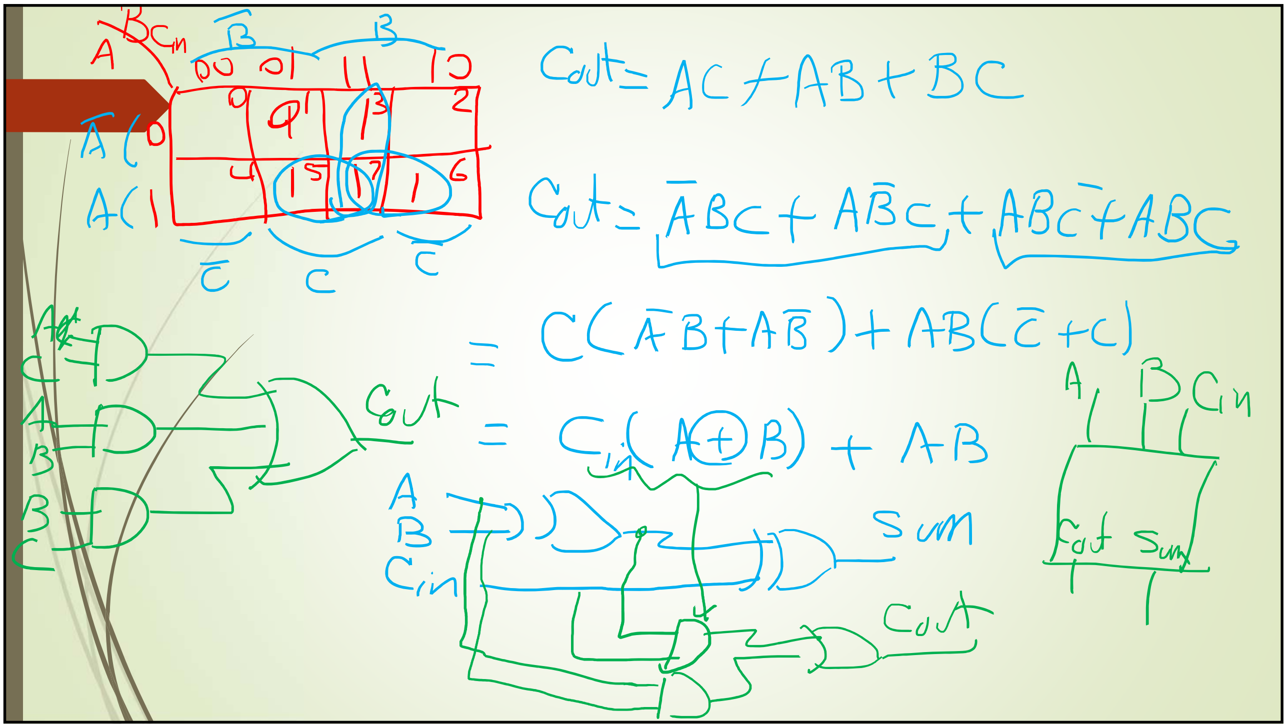

$Sum = \overline{A}\,\overline{B}C + \overline{A}B\overline{C}$
$A\overline{B}\,\overline{C} + ABC$

$Sum = \overline{A}(\overline{B}C + B\overline{C}) + A(\overline{B}\,\overline{C} + BC)$

$= \overline{A}(B \oplus C) + A(\overline{B \oplus C})$

$= \overline{A}X + A\overline{X}$

$= A \oplus X \rightarrow A \oplus B \oplus C$



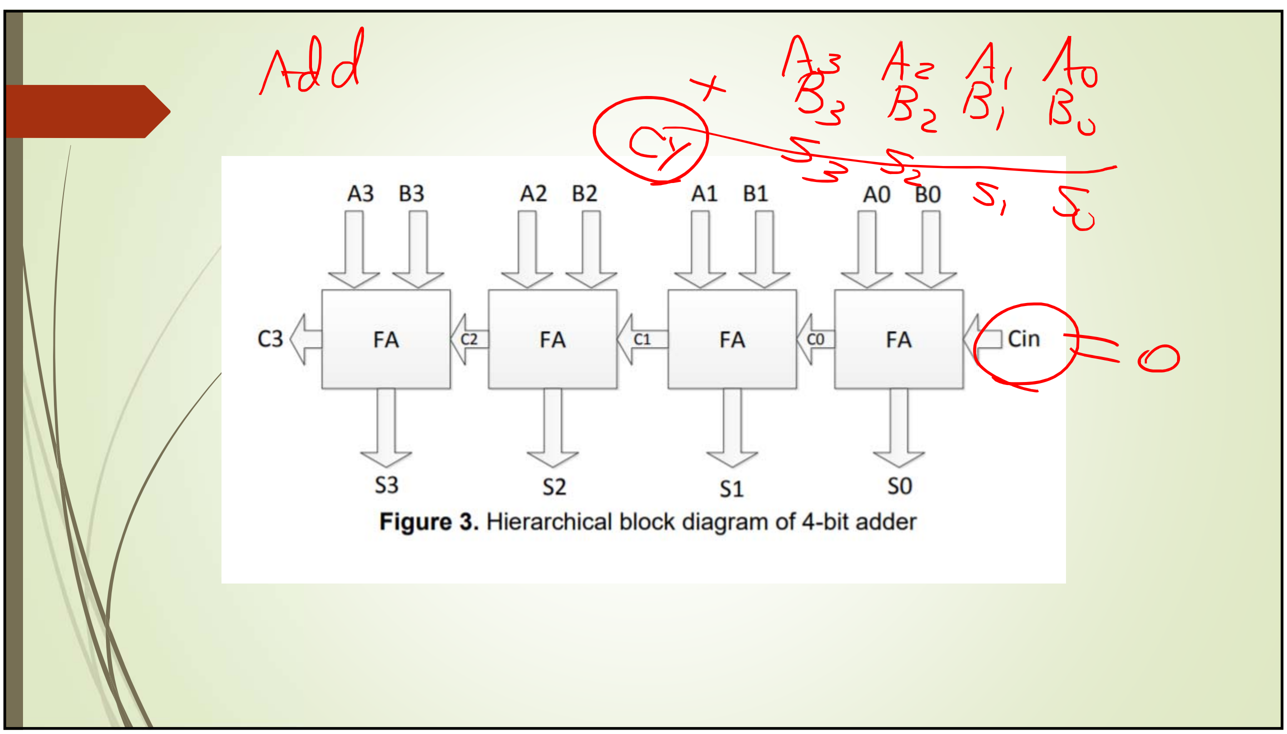




**Figure 3.** Hierarchical block diagram of 4-bit adder

Subtract A − B

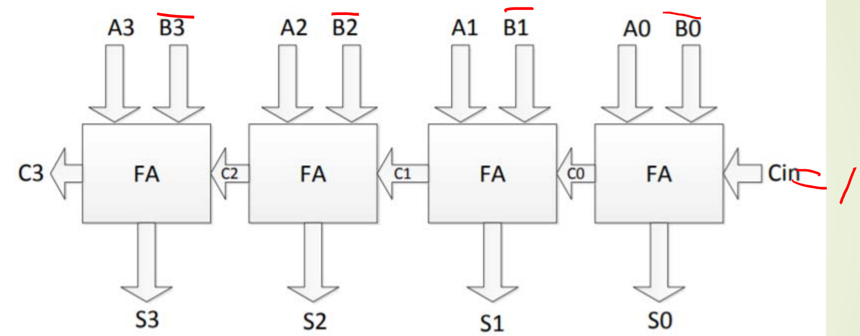



**Figure 3.** Hierarchical block diagram of 4-bit adder

$$x \oplus y = \bar{x}y + x\bar{y}$$

$$0 \oplus y = y$$

$$1 \oplus y = \bar{y}$$

# Four-bit adder-subtractor (with overflow detection)