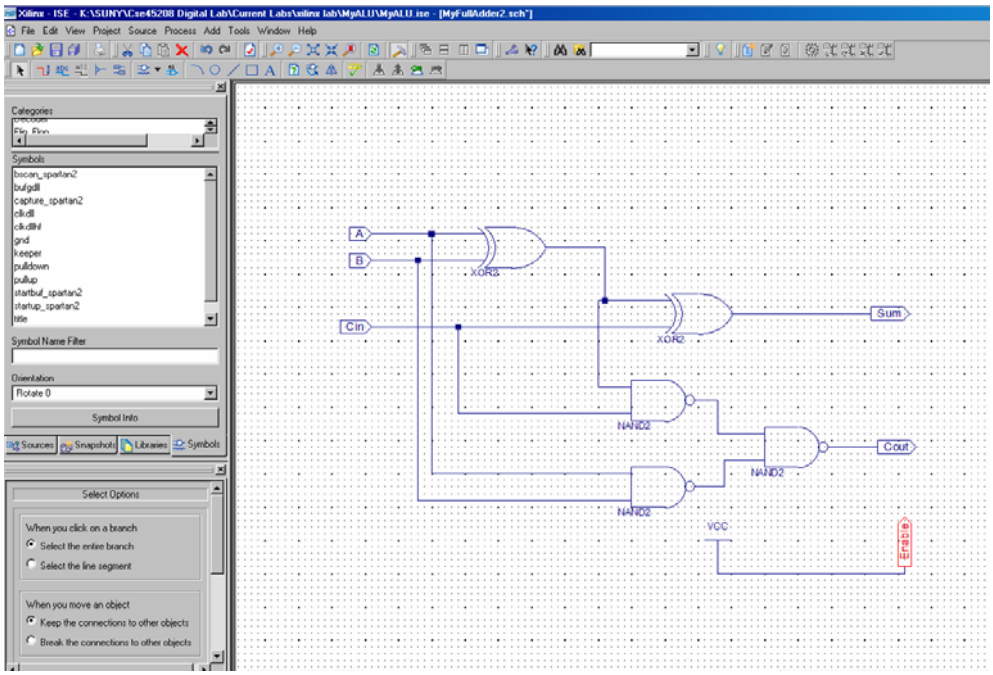
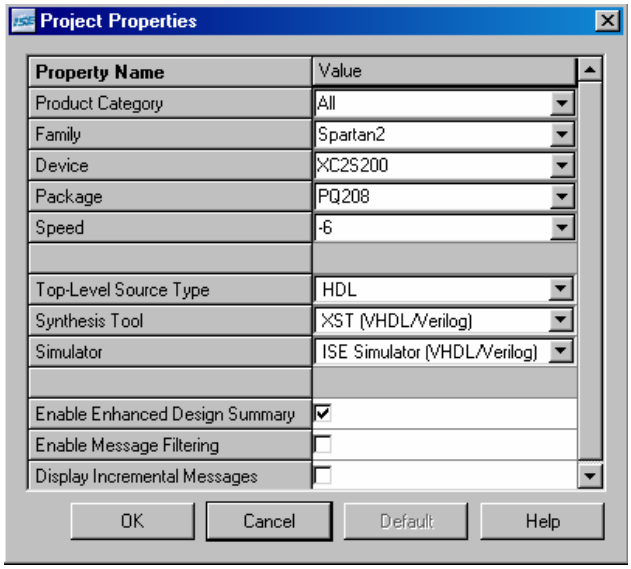
Tutorial
Xilinx ISE Download to Digilab II Board Simulator
<Release Version: 8.2i>

Department of Electrical and Computer Engineering
State University of New York – New Paltz

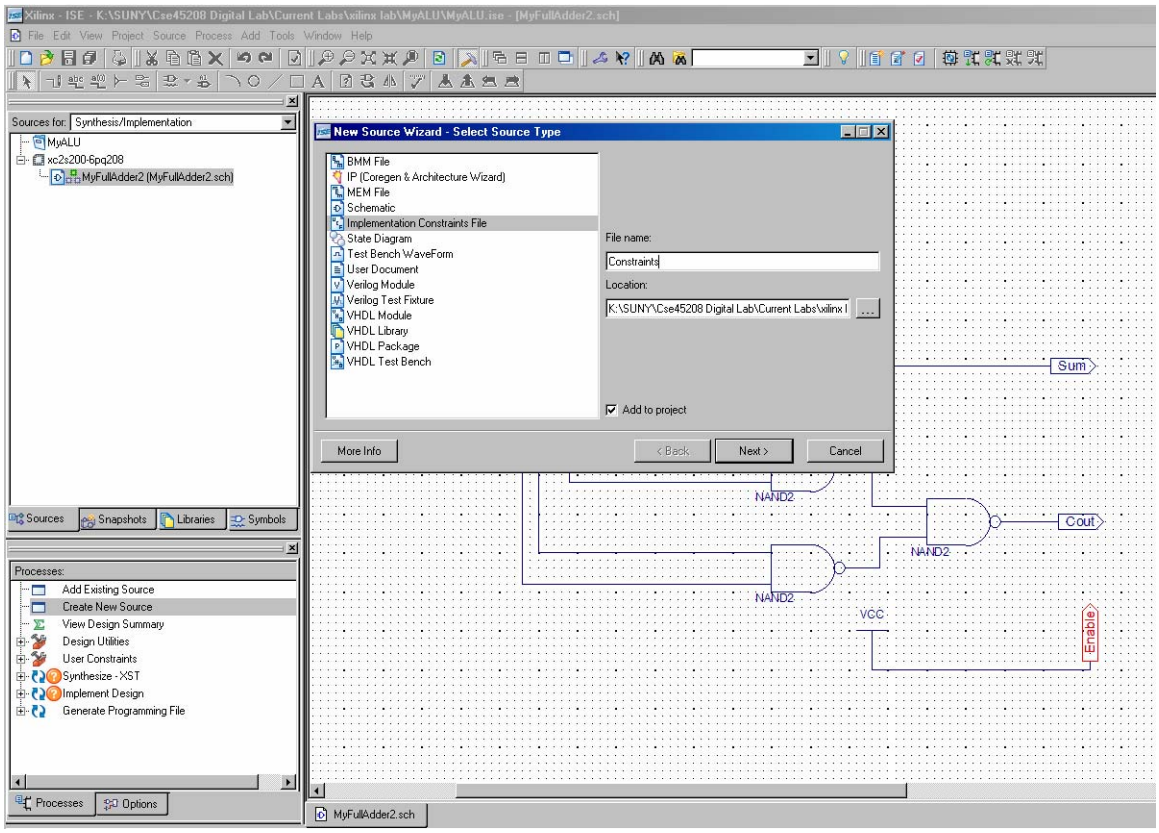
Now that through simulation you have verified that your design is working, the next step is to download your design into the FPGA (Field Programmable Gate Array) of the Digilab II Board. On the highest level of your design hierarchy add an extra output and connect it to the Vcc. Vcc is located in the **General** category. This is needed to enable the LEDs on the board. Let's name the output Enable. Save your schematic and return to the Project Navigator.



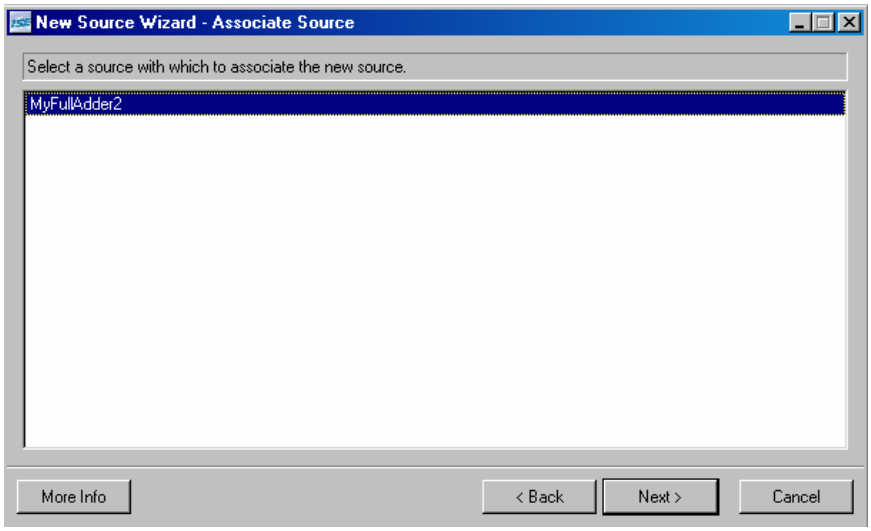
Before proceeding, once again make sure that the FPGA device under sources is listed as XCS2S200-6pq208. If not double click on the device and make corrections as follows



Now under Sources window, use the drop box to select Synthesis/Implementation. Then, select the schematic to be downloaded and double click on Create New Source under Processes. This will open a dialog box. Select Implementation Constraints File, enter a file name and click Next.

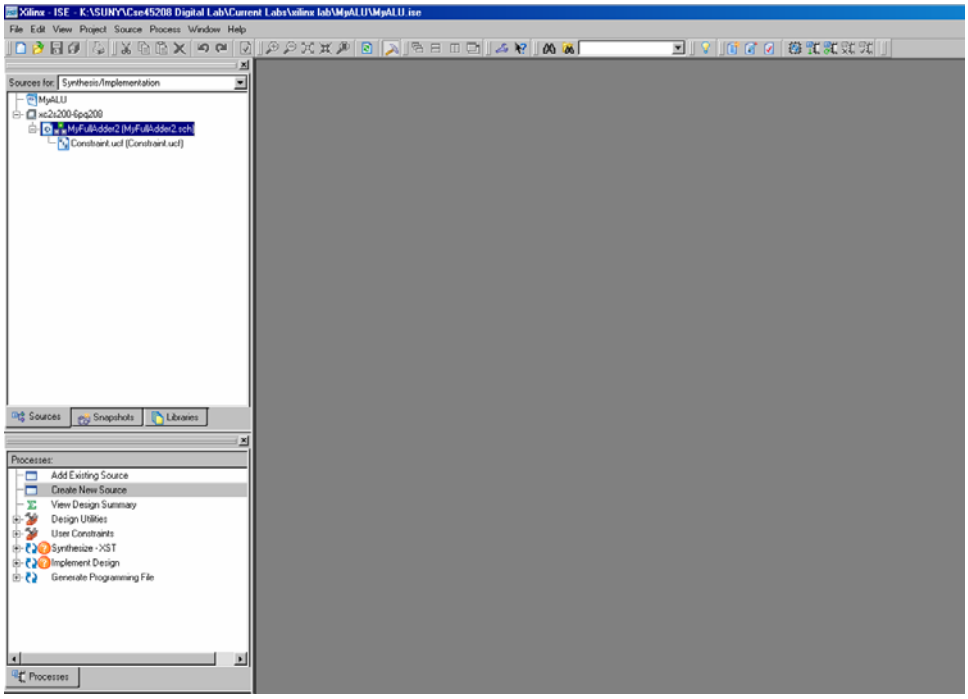


This opens up the following dialog box in which select the appropriate source for which the constraints file is being created.

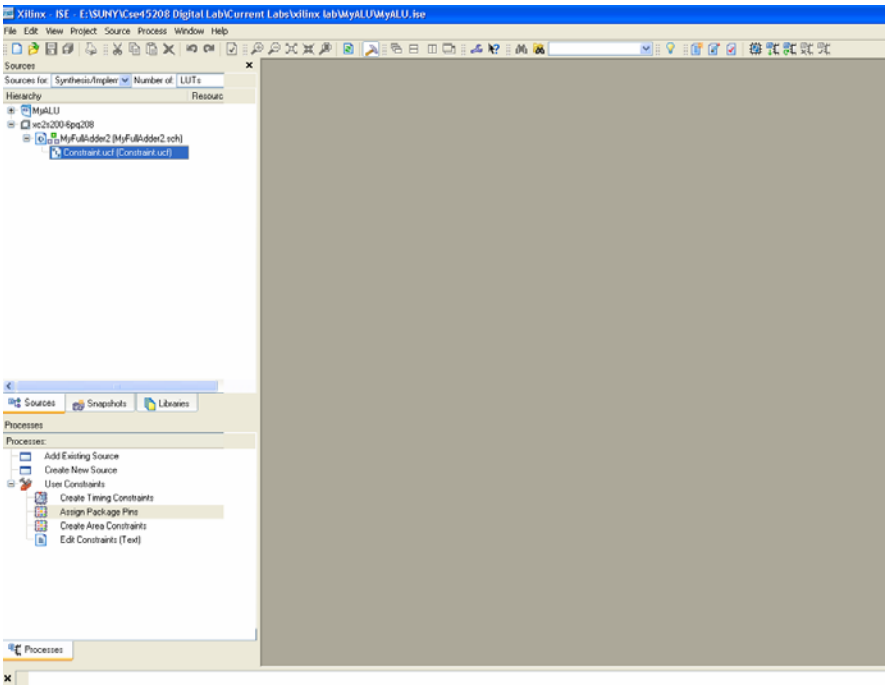


Click Next! And then Finish!

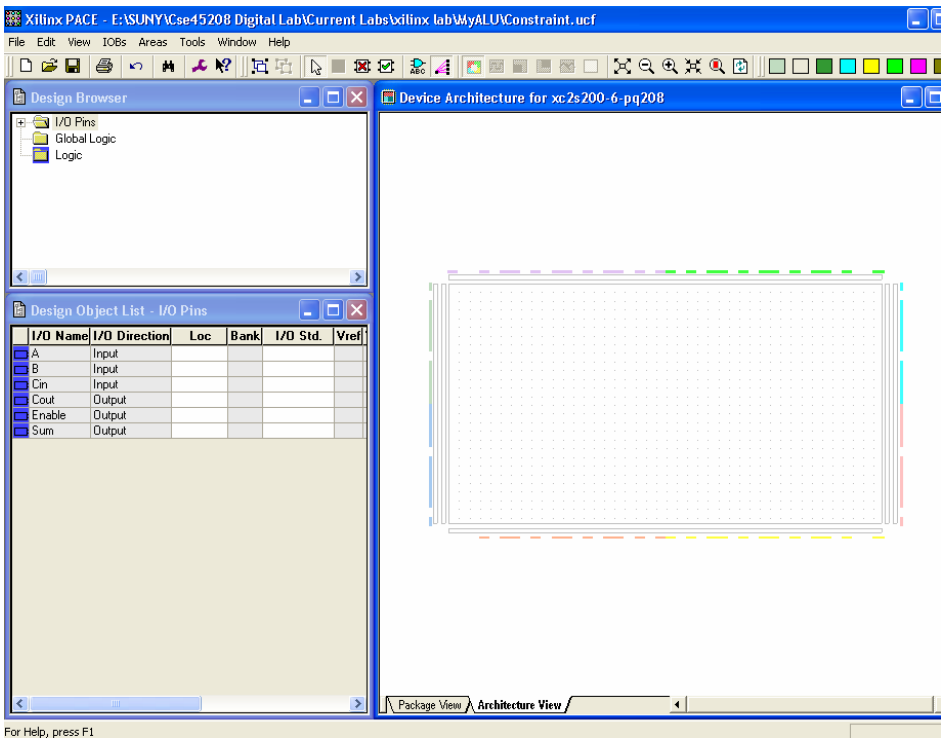
The constraints file, constraints.ucf has been created



Click on the UCF file and in the Processes window, under User Constraints, double click on Assign Package Pins.



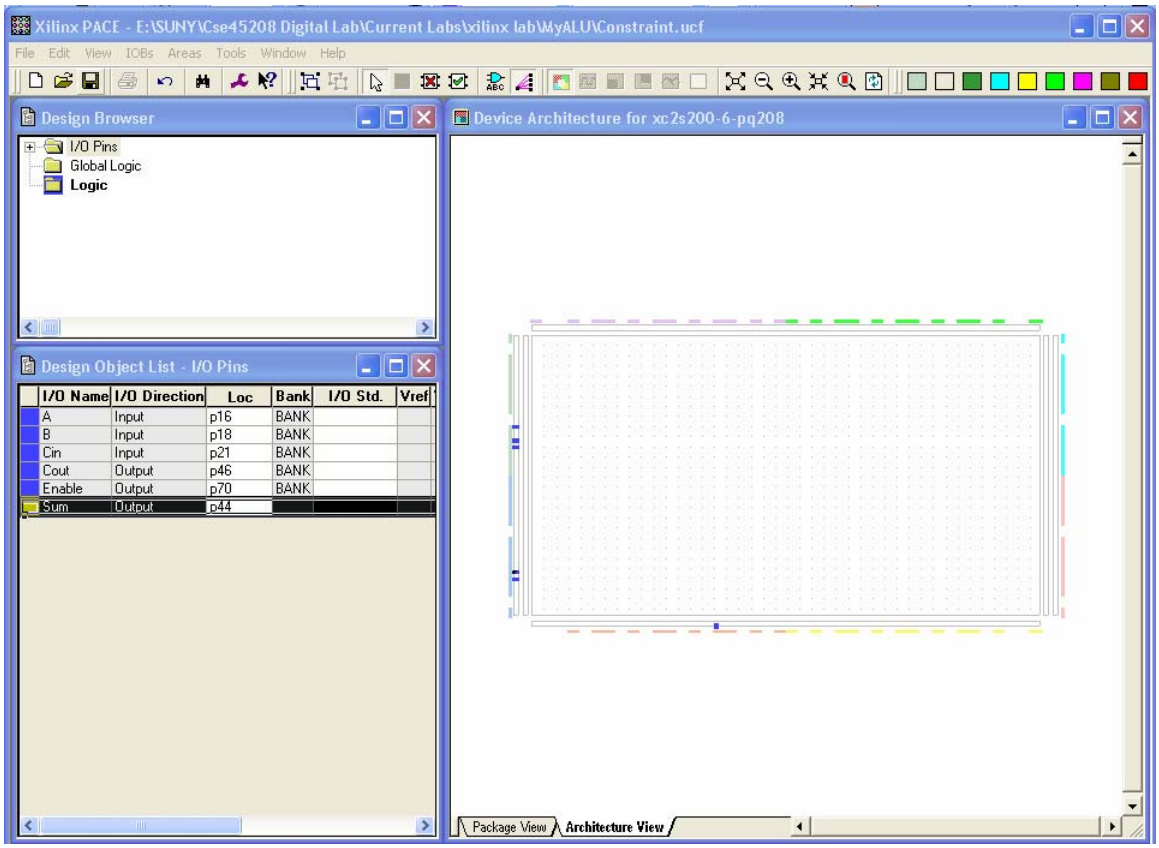
This opens the following Constraints Editor. In the ***Design Object List – I/O Pins*** window, we will physically assign the inputs and outputs to the pins of the FPGA per assignment in the Interconnect Table at the end of this tutorial.



The three inputs (A, B, Cin) need to be assigned to switches. Let's pick the first three switches. The locations of the first three switches (SW1, SW2, SW3) are at locations P16, P18, P21 respectively.

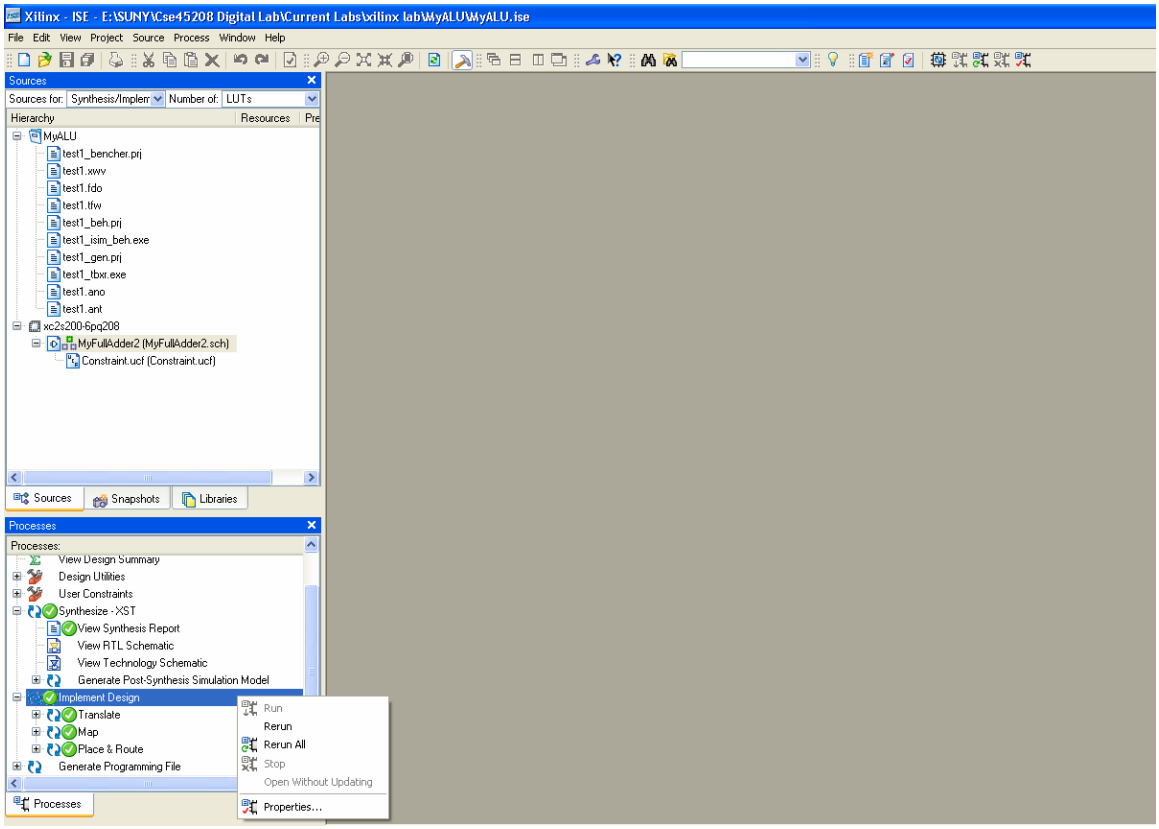
The two outputs (S, Cout) need to be assigned to LEDs. Let's pick the first two LEDs. The locations for the LEDs (LD1 and LD2) are P44 and P46.

The output Enable needs to be assigned to P70 for every project. Assign the pin numbers for the inputs (A, B, Cin) and the outputs (S, Cout and Enable)

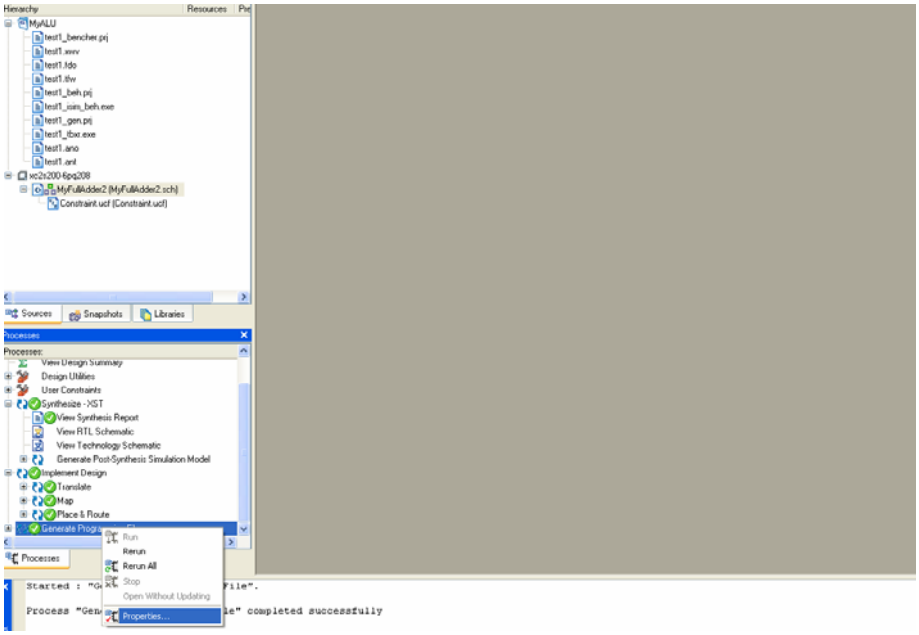


Save the changes and close. Return to the project navigator.

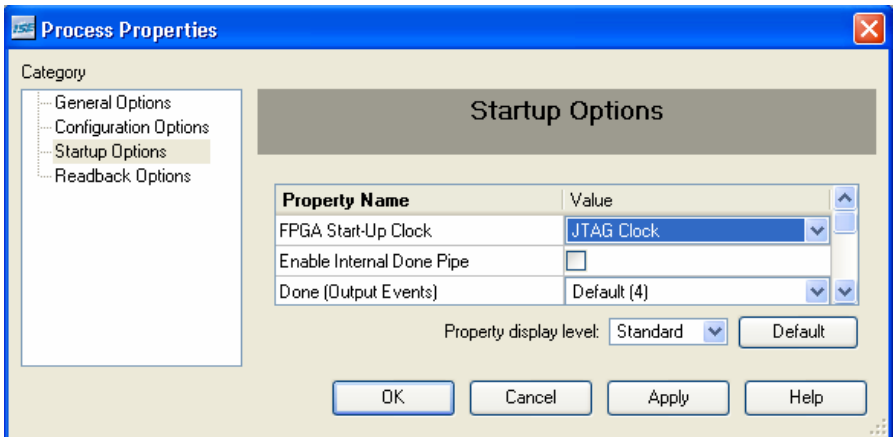
Double click on Implement Design (or right click on Implement Design -> Rerun).



If there are no errors generated the next step is to create a BIT file. Right click on Generate Programming File -> Properties.

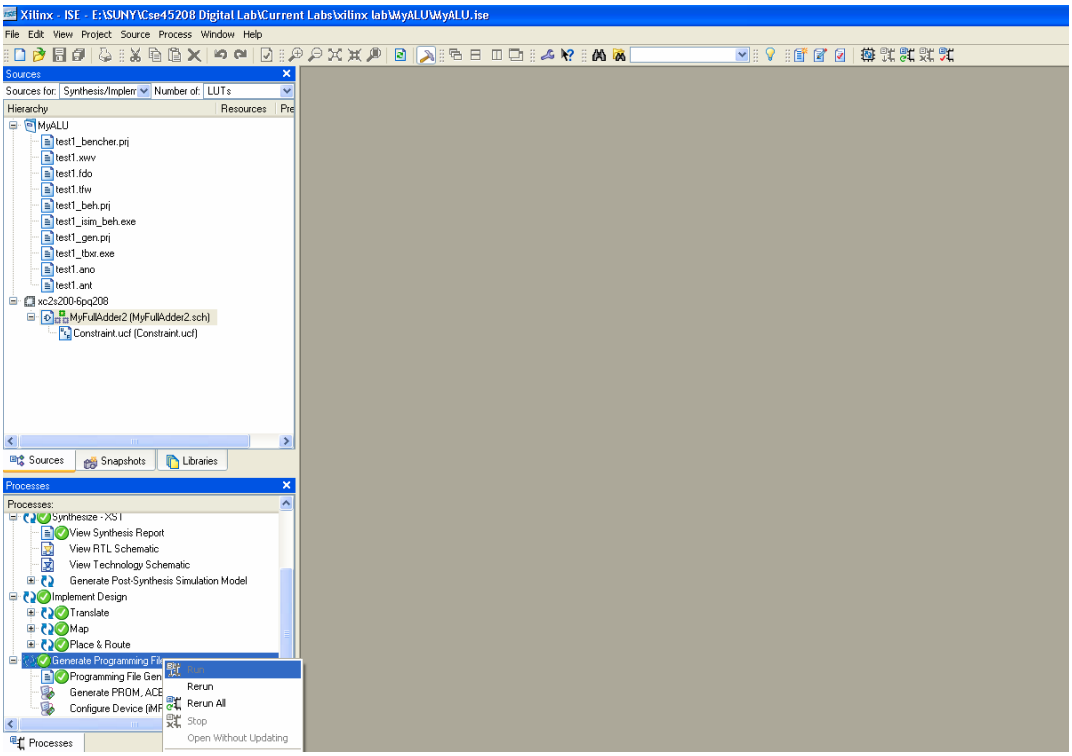


Click the Startup Options tab. And change the Start-Up Clock to JTAG Clock.



Click Ok.

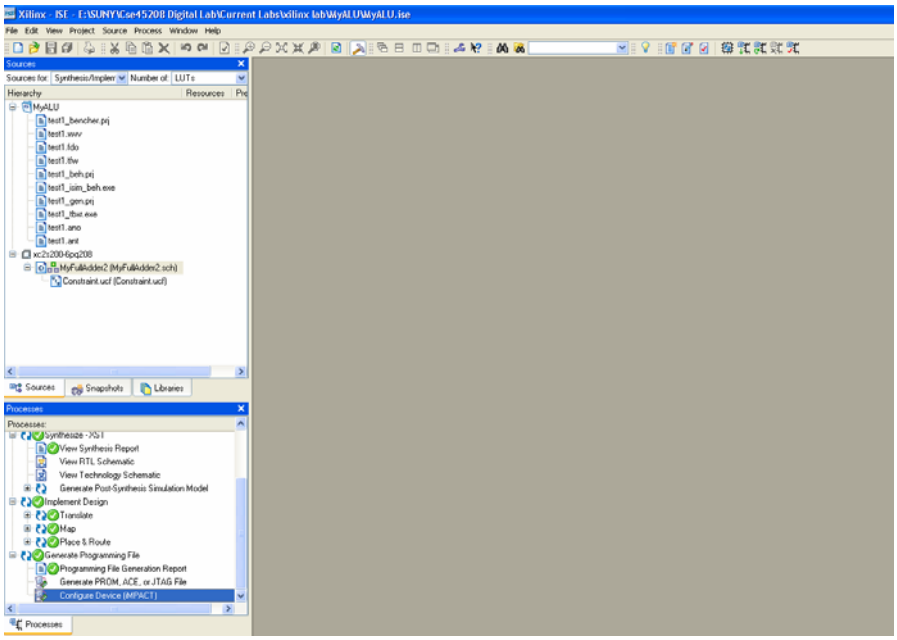
Double click on Generate Programming File (or alternatively, right click on Generate Programming File -> Run).



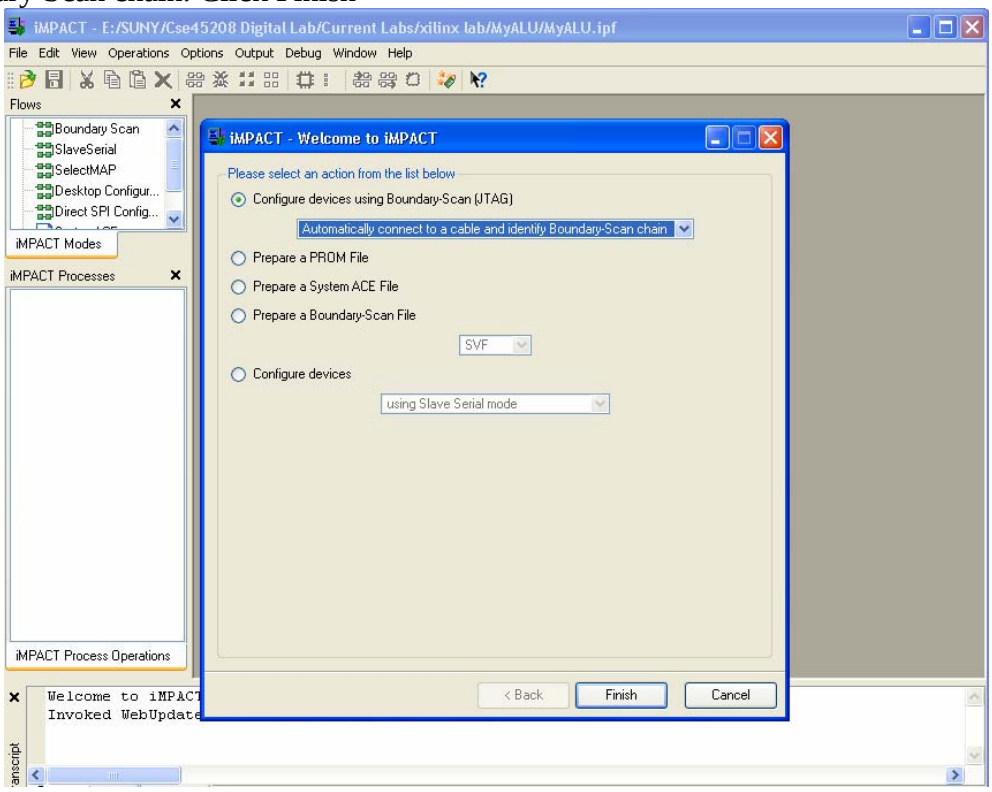
Now your BIT file is ready to be downloaded to the Digilab 2 board.

Make sure that the DIO1 board (the smaller one) is connected into tabs E & F of the Digilab 2 board (the larger one). Connect the power supply to the board before you plug the supply to the outlet. Once the power supply is connected and powered up, connect the parallel port to the computer first, then to the board. There is a small switch next to the parallel port on the board. The switch must be in the JTAG position. If it is not in this position then Xilinx will not find the board.

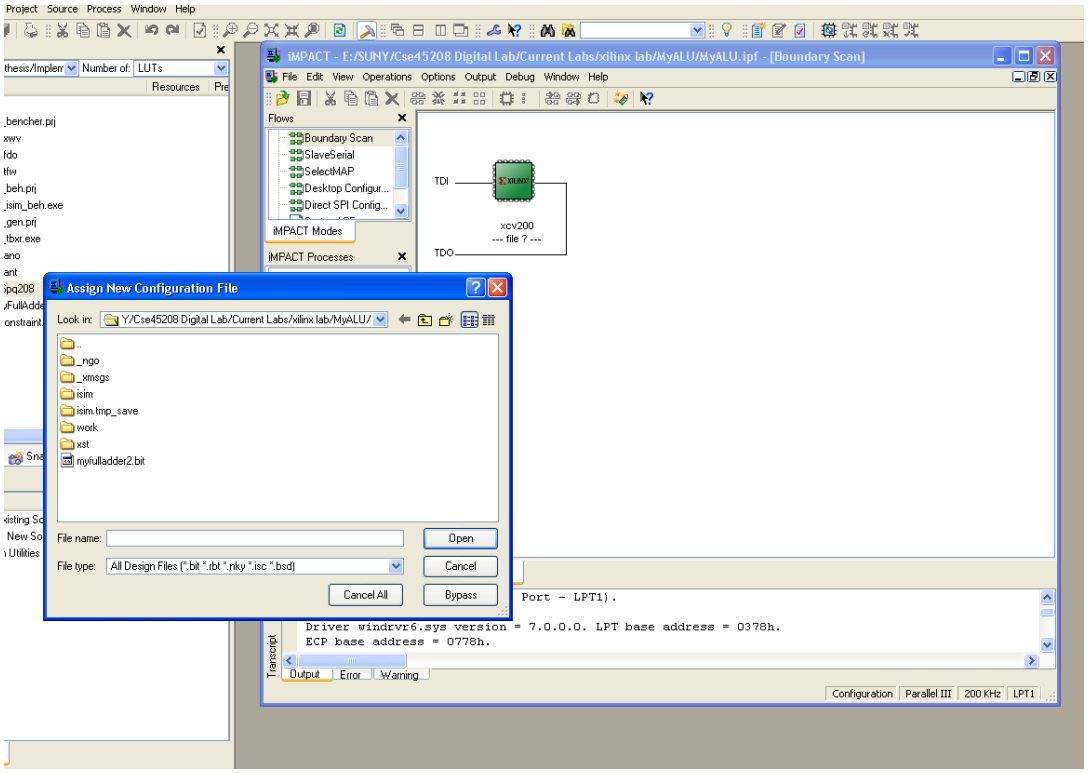
Now it is time to download. Return to the Project Navigator. Double click Generate Programming File -> Configure Device (iMPACT)



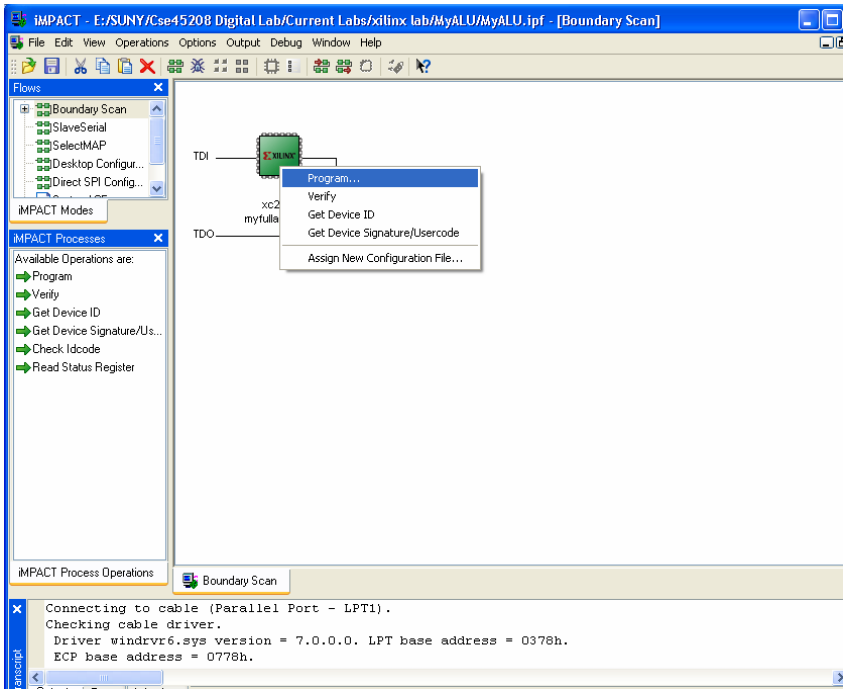
This will open up the following dialog box , Select Configure devices using Boundary Scan (JTAG) and in the drop box choose automatically connect to a cable and identify Boundary Scan chain. Click Finish



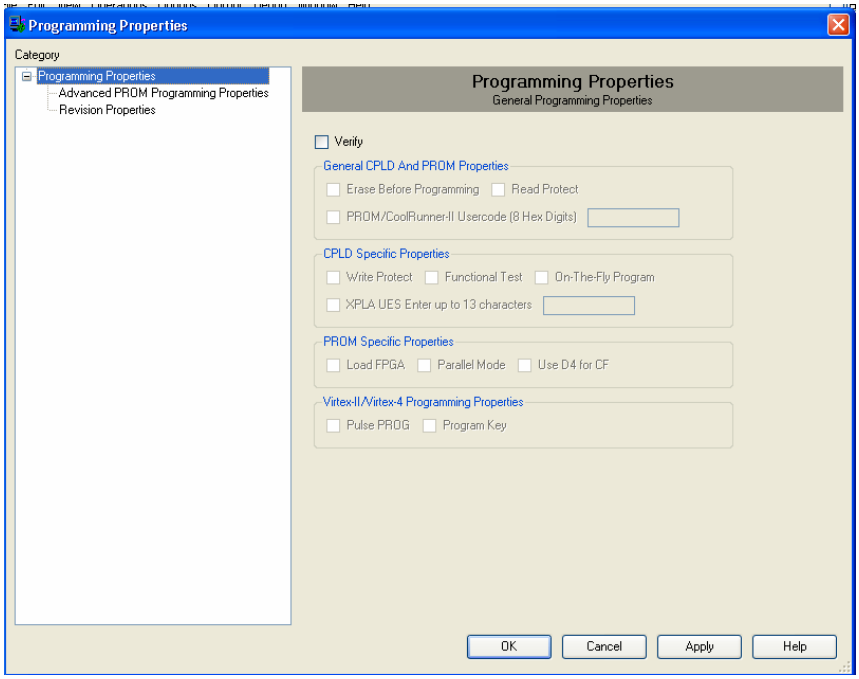
If the board is not connected properly, it will generate an error saying that it cannot connect to the board. If it finds the board then you will get the following.



Select your bite file (*filename*.bit) and click Open. Next, right click on the device and choose Program.

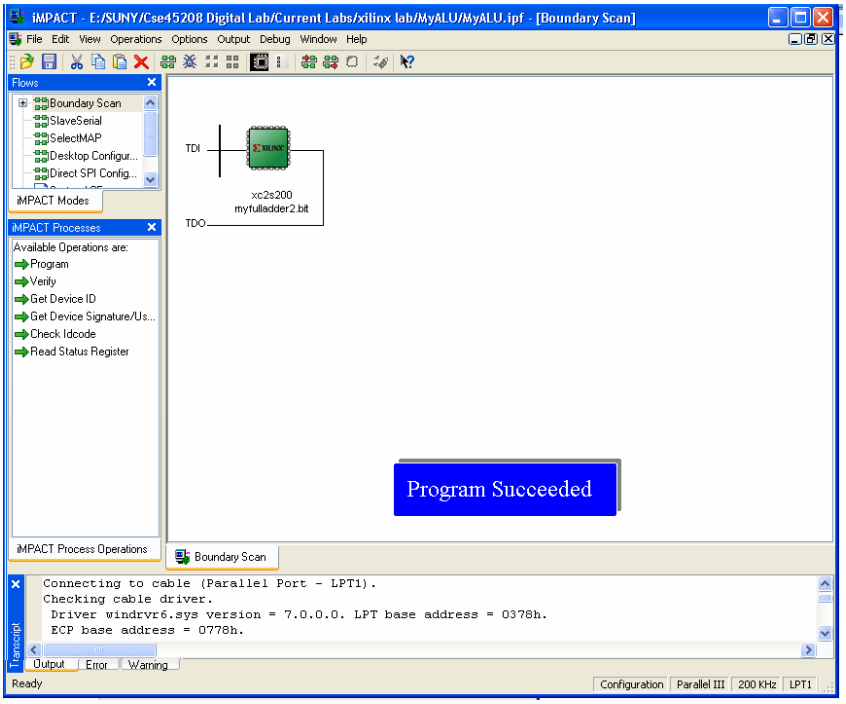


The following window will open.



Click Ok. And the BIT file will begin to download.

If everything is successful, you will get the following message.



Now flip the switches on the board, and see your design come to life!

SUGGESTIONS FOR ALU

For the ALU we suggest that you use the following switches for each of the 11 inputs.

- *DATA A*

A is a four-bit bus. Therefore, four switches will be needed.

A(3) -> SW1 -> P16
A(2) -> SW2 -> P18
A(1) -> SW3 -> P21
A(0) -> SW4 -> P23

- *DATA B*

B is also a four-bit bus.

A(3) -> SW5 -> P27
A(2) -> SW6 -> P30
A(1) -> SW7 -> P33
A(0) -> SW8 -> P35

- *SELECT LINES*

There are three select lines. We will use the push buttons.

SW(2) -> BTN1 -> P37
SW(1) -> BTN2 -> P41
SW(0) -> BTN3 -> P42

- *OUTPUTs*

There are four data outputs, and four "extra" outputs.

DATA(3) -> LD1 -> P44
DATA(2) -> LD2 -> P46
DATA(1) -> LD3 -> P48
DATA(0) -> LD4 -> P57

Z -> LD5 -> P59
OF -> LD6 -> P61
N -> LD7 -> P63
C -> LD8 -> P68

Digilab Digital I/O 1, Rev B to Digilab D2

DIO1B Pin	Signal	D2 Pin	Signal	FPGA Pin
A1		B39		
A2		B40		
A3		B37		
A4		B38		
A5		B35		
A6		B36		
A7		B33		
A8		B34		
A9		B31		
A10		B32		
A11		B29		
A12		B30		
A13		B27		
A14		B28		
A15		B25		
A16		B26		
A17		B23		
A18		B24		
A19		B21		
A20		B22		
A21		B19		
A22		B20		
A23		B17		
A24		B18		
A25		B15		
A26		B16		
A27		B13		
A28		B14		
A29		B11	B11	185
A30		B12	B12	182
A31	BLU	B9	B9	188
A32	PS2D	B10	B10	187
A33	GRN	B7	B7	191
A34	PS2C	B8	B8	189
A35	RED	B5	B5	193
A36	HS	B6	B6	192
A37	VCC	B3	VCC	
A38	VS	B4	B4	194
A39	GND	B1	GND	
A40	VU	B2	VU	

DIO1B Pin	Signal	D2 Pin	Signal	FPGA Pin
B1	CA	A39	A39	17
B2	SW1	A40	A40	16
B3	CB	A37	A37	20
B4	SW2	A38	A38	18
B5	CC	A35	A35	22
B6	SW3	A36	A36	21
B7	CD	A33	A33	24
B8	SW4	A34	A34	23
B9	CE	A31	A31	29
B10	SW5	A32	A32	27
B11	CF	A29	A29	31
B12	SW6	A30	A30	30
B13	CG	A27	A27	34
B14	SW7	A28	A28	33
B15	DP	A25	A25	36
B16	SW8	A26	A26	35
B17	BTN2	A23	A23	41
B18	BTN1	A24	A24	37
B19	BTN4	A21	A21	43
B20	BTN3	A22	A22	42
B21	A1	A19	A19	45
B22	LD1	A20	A20	44
B23	A2	A17	A17	47
B24	LD2	A18	A18	46
B25	A3	A15	A15	49
B26	LD3	A16	A16	48
B27	A4	A13	A13	58
B28	LD4	A14	A14	57
B29		A11	A11	60
B30	LD5	A12	A12	59
B31		A9	A9	62
B32	LD6	A10	A10	61
B33		A7	A7	67
B34	LD7	A8	A8	63
B35	BTN5	A5	A5	69
B36	LD8	A6	A6	68
B37	VCC	A3	VCC	
B38	LDG	A4	A4	70
B39	GND	A1	GND	
B40	VU	A2	VU	