New Paltz
STATE UNIVERSITY OF NEW YORK

Division of Engineering Programs

EGC220 Digital Logic Fundamentals

Test 2

For full credit, you need to show your work.
Closed Book and Notes

First Name: KEY **Last Name:** _____

- For full credit, you need to show complete work and answer the questions as directed.
- Your submission must be in a single PDF file
- Make sure you submit before the deadline of 3:15 PM. I will not accept late submission by email.
- You must adhere to the honor code. Any evidence of misconduct will be dealt with strictly per syllabus.

20 PT.

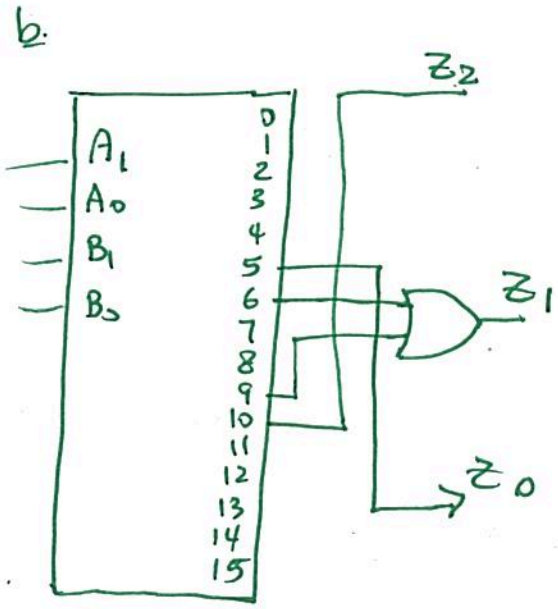
1)

a. Develop the truth table only of a combinational circuit that multiplies A × B, where A and B are multi-bit inputs. The range of input A is from 1 to 2 and the range of input B is from 0 to 2. → 2x2 = 4

b. Implement the design using a decoder and external OR gates.

A_1	A_0	B_1	B_0	Z_2	Z_1	Z_0
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0	0	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	X	X	X
1	0	0	0	0	0	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	X	X	X
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

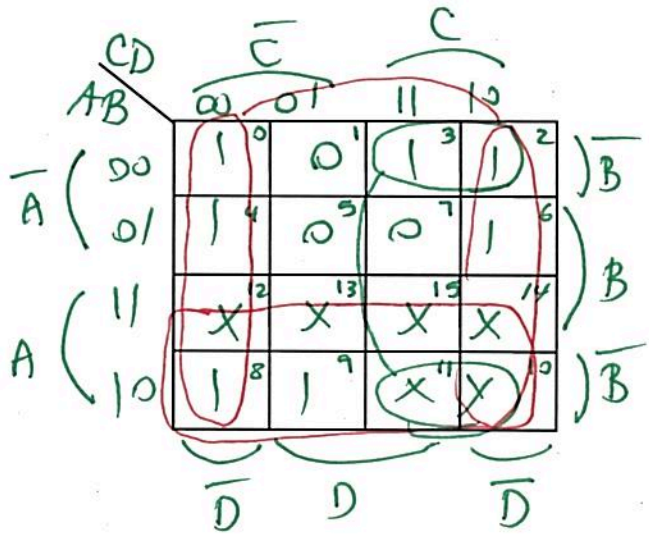
b.



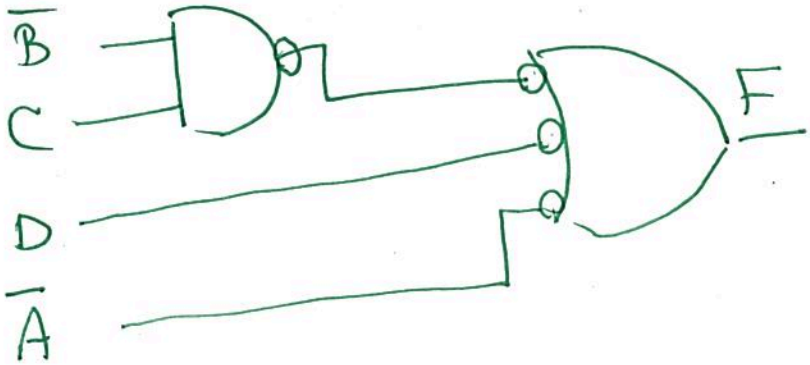
20 PT.

2) Design an all-NAND circuit that has 4 inputs, labeled A, B, C and D, and one output F. The output is 1 if and only if the <u>BCD input</u> combination is divisible by 3 (dividing the number by 3 will result in 0 remainder) or divisible by 2 i.e. 0101 represents 5 which is not divisible by 3 or by 2 (F =0) and 1001 represents 9, which is divisible by 3 (F=1), even though it is not divisible by 2. 0 is technically divisible both by 3 and 2.

ABCD	F
0000	1
0001	0
0010	1
0011	1
0100	1
0101	0
0110	1
0111	0
1000	1
1001	1
1010	X
1011	
1100	
1101	
1110	
1111	



$F = A + \bar{D} + \bar{B}C$

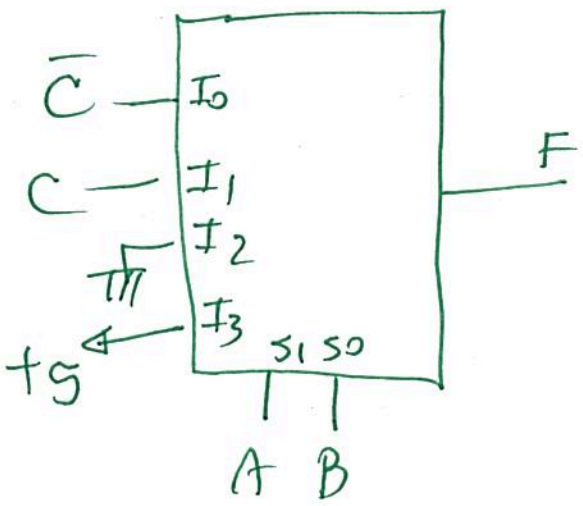


15 PT.

3) Using a 4 × 1 multiplexer, design a circuit for the following function. Assign A and B to the select lines.

$$F(A,B,C) = \sum m\,(0, 3, 6, 7)$$

A	B	C	F	
0	0	0	1	$\bar{C}$
0	0	1	0	
0	1	0	0	C
0	1	1	1	
1	0	0	0	ϕ
1	0	1	0	
1	1	0	1	1
1	1	1	1	

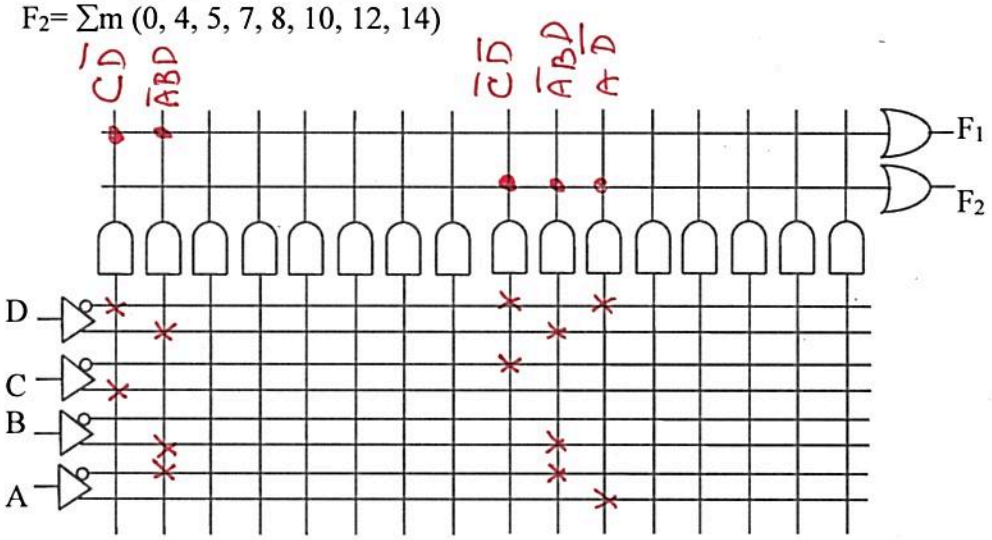


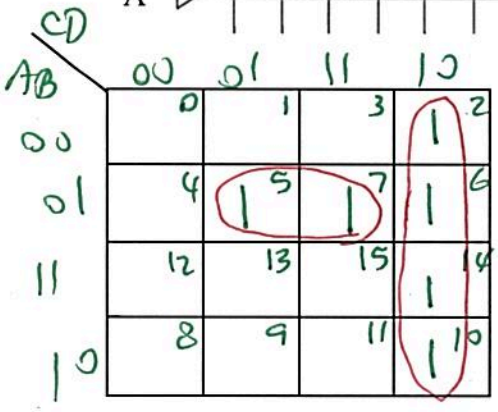
15 PT.

4) Implement the following functions using a PAL (programmable AND array and Fixed OR array). Make sure to mark each fixed connection with ● and each fused connection with ×.

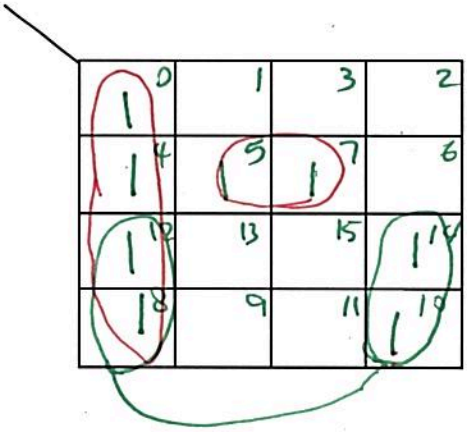
$F_1 = \sum m\ (2, 5, 6, 7, 10, 14)$

$F_2 = \sum m\ (0, 4, 5, 7, 8, 10, 12, 14)$





$F_1 = C\bar{D} + \bar{A}BD$

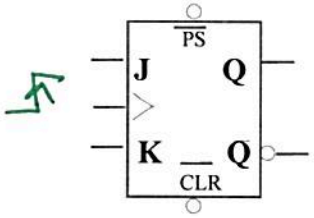


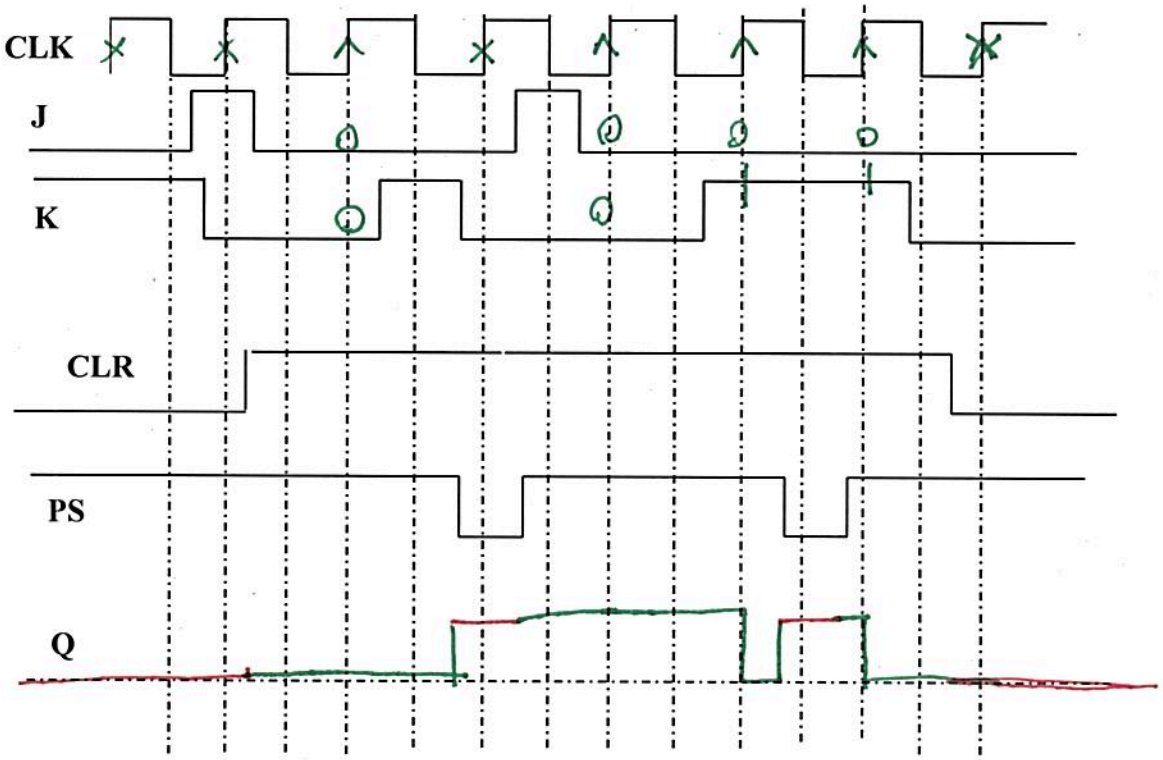
$F = \bar{C}\bar{D} + \bar{A}BD + A\bar{D}$

15 PT.

5) Complete the following timing diagram for the given device.

J	K	Q(t+)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$





15 PT.

6) Using S-R flip-flops, design a ripple counter that counts from 3 to 5 and repeat.