EGC220 Quiz #24 Dr. Izadi

First NAME: Key Last Name: _____

25 Points

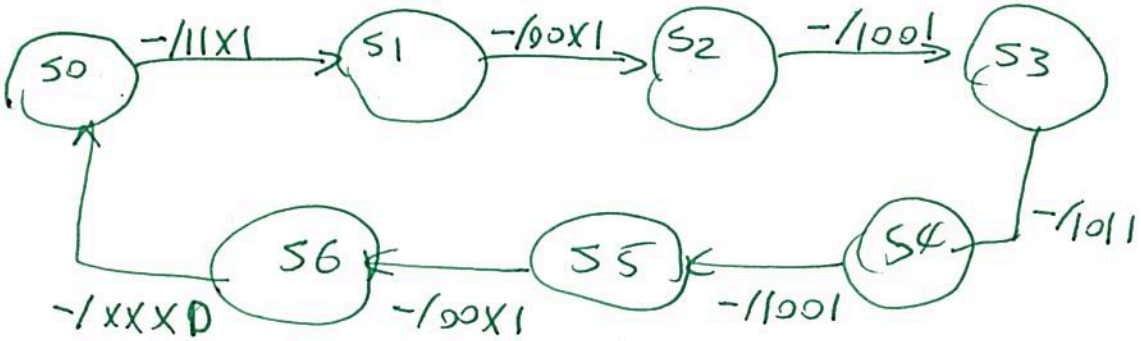
Problem 1

Develop the state diagram ONLY of a Mealy based controller to generate the following sequence at the output of 74194. Make sure you explicitly identify your outputs i.e. S_1 S_0 CLR A B ….

	S_1	S_0	SIL	SIR	A	B	C	D	CLR
0001	1	1	X	X	0	0	0	1	1
0001	0	0	X	X	X	X	X	X	1
0010	1	0	0	X	X	X	X	X	1
0101	1	0	1	X	X	X	X	X	1
1010	1	0	0	X	X	X	X	X	1
1010	0	0	X	X	X	X	X	X	1
0000	X	X	X	X	X	X	X	X	0

S_1 S_0	
00	NC
01	SR
10	SL
11	LD

S_1 S_0 SIL CLR

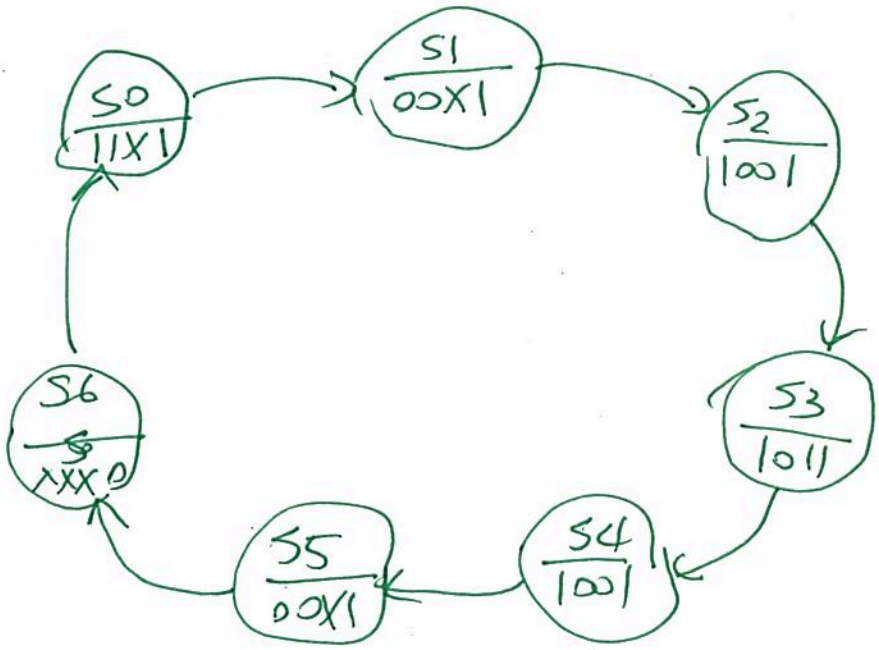


25 Points

Problem 2

Develop the state diagram ONLY of a Moore based controller to generate the following sequence at the output of 74194. Make sure you explicitly identify your outputs i.e. S_1 S_0 CLR A B ….

0001
0001
0010
0101
1010
1010
0000



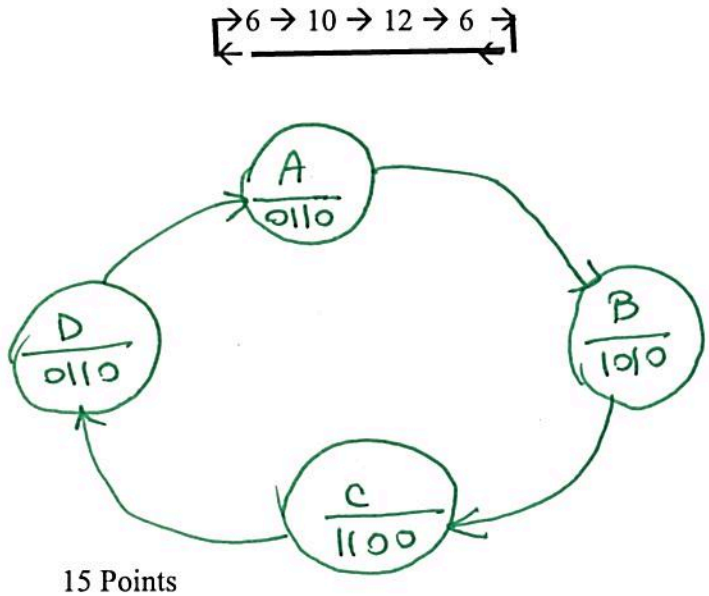
EGC220 Quiz #23 *Dr. Izadi*

First NAME: Key Last Name:_____

15 Points

Problem 1

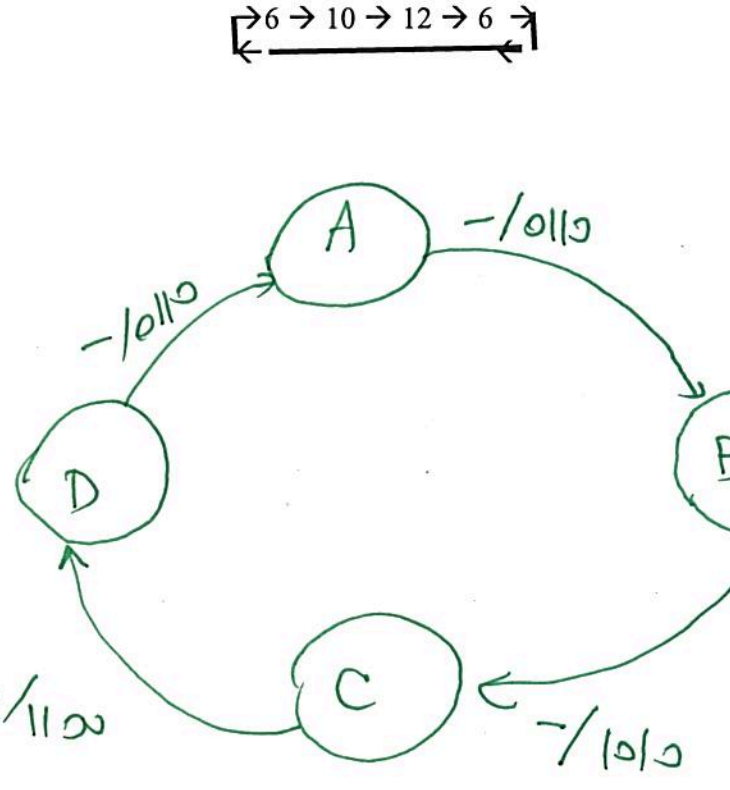
Develop the state diagram only of a Moore based state machine to generate the given sequence.



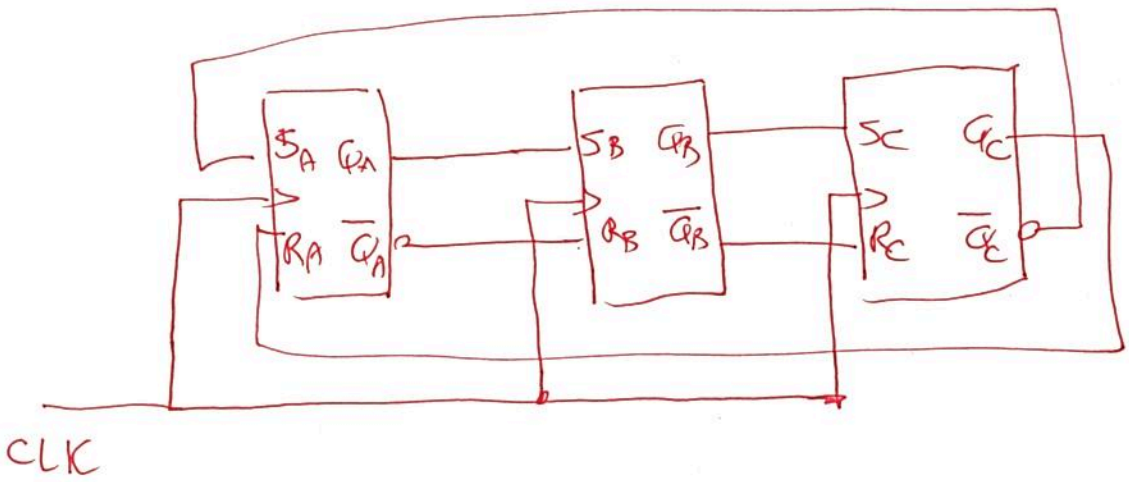
15 Points

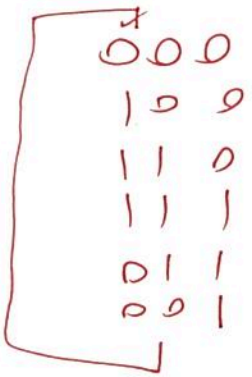
Problem 2

Develop the state diagram only of a Mealy based state machine to generate the given sequence.



20 Points
Problem 3
Design a Mod 6 Johnson Counter using SR flip-flops. Is the design race free? Why?





only 1 FF changes per transitio

EGC220 Quiz #22 Dr. Izadi

First NAME: Key Last Name:

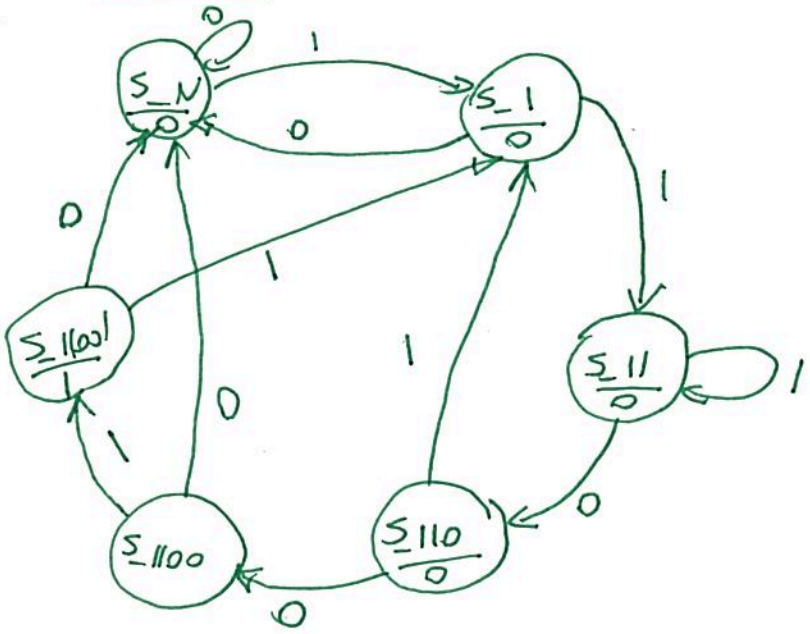
Problem 1

Show the state diagram only of a Moore based sequence detector with one input and one output. The output should generate an output of 1 only when the input sequence is 11001 is detected. Assume no overlapping of sequences: i.e., 110011001 generates 0000100000.

S_N

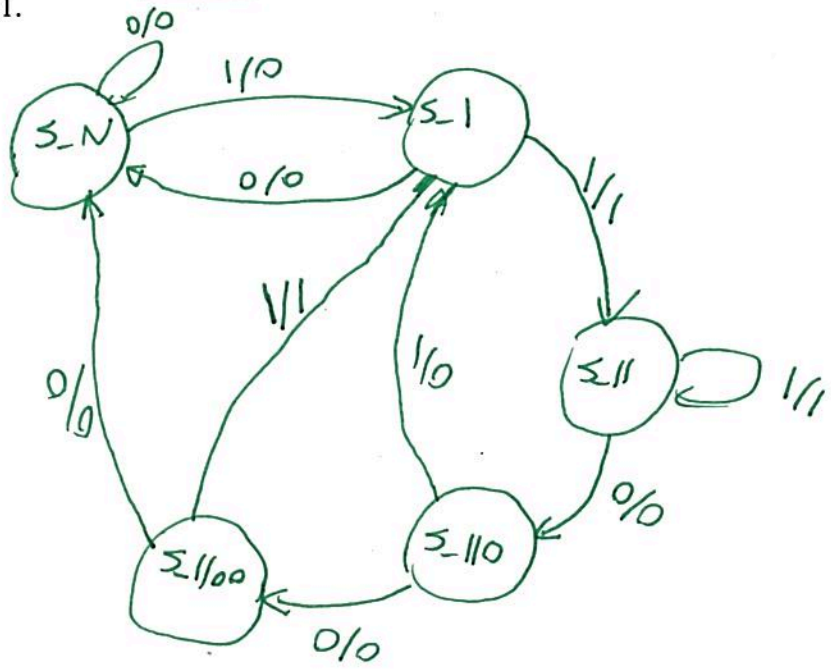
S_1 = 1

S_11: 11



Problem 2

Show the state diagram only of a Mealy based sequence detector with one input and one output. The output should generate an output of 1 only when the input sequence is 11001 is detected. Assume overlapping of sequences allowed i.e., 110011001 generates 000010001.

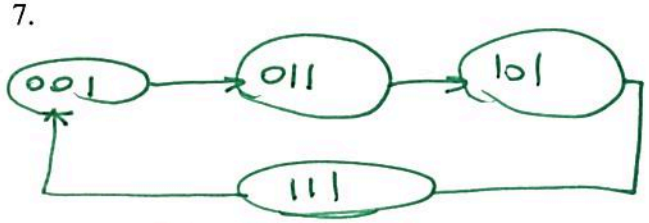


EGC220 Quiz #21 *Dr. Izadi*

First NAME: Key Last Name: _____

Using D flip-flops, design a counter with the following repeated binary sequence: 1, 3, 5, 7.

I.



$Q_A(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

Q_A	Q_B	Q_C	D_A	D_B	D_C
0	0	0	X	X	X
0	0	1	0	1	1
0	1	0	X	X	X
0	1	1	1	0	1
1	0	0	X	X	X
1	0	1	1	1	1
1	1	0	X	X	X
1	1	1	0	0	1

Q_A \ $Q_B Q_C$	00	01	11	10
0	X	0	1	X
1	X	1	0	X

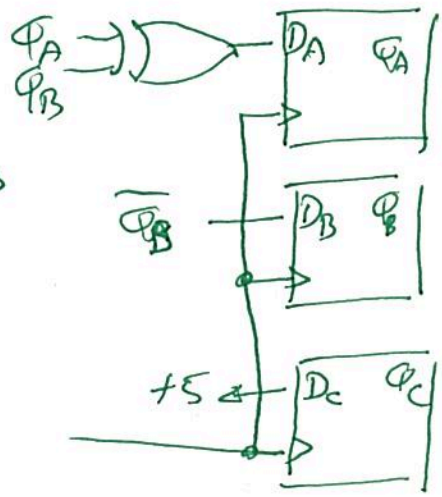
$D_A = Q_A\bar{Q}_B + \bar{Q}_A Q_B$

$= Q_A \oplus Q_B$

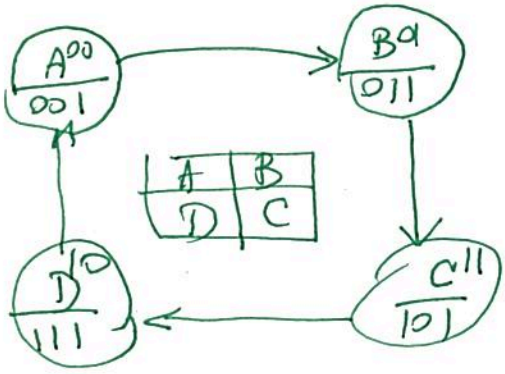
Q_A \ $Q_B Q_C$	00	01	11	10
0	X	1	0	X
1	X	1	0	X

$D_B = \bar{Q}_B$

$D_C = 1$



II.



Q_A	Q_B	$N S$ Q_A	Q_B	Z_2	Z_1	Z_0
0	0	0	1	0	0	1
0	1	1	1	0	1	1
1	0	0	0	1	1	1
1	1	1	0	1	0	1

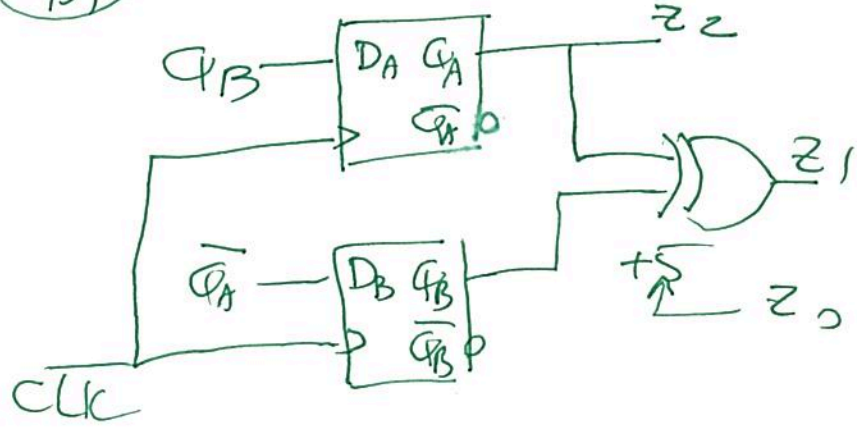
$D_A = Q_B$

$D_B = \bar{Q}_A$

$Z_2 = Q_A$

$Z_1 = Q_A \oplus Q_B$

$Z_0 = 1$

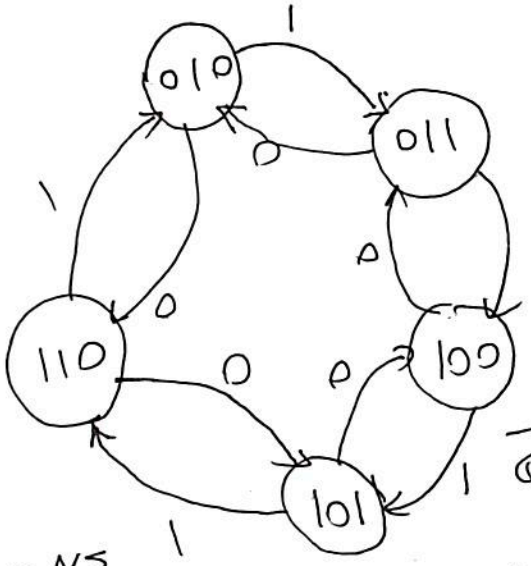


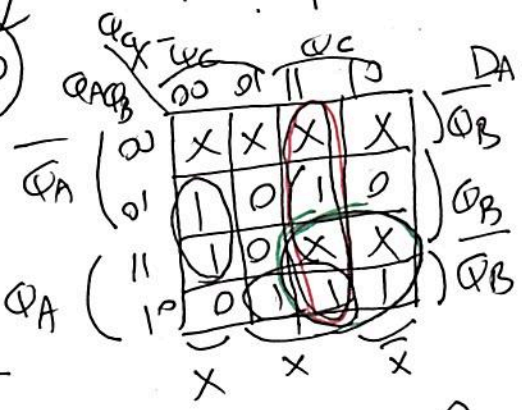
EGC220 Quiz #20 *Dr. Izadi*

First NAME: Key Last Name: _____

Problem 1

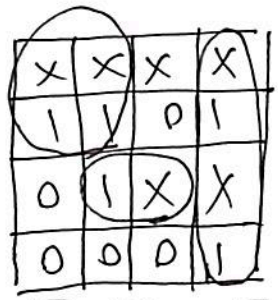
Using D flip-flops, design a 2 to 6 up/down counter: for x=1, it will count 2 to 6 and for x=0, it will count 6 to 2.



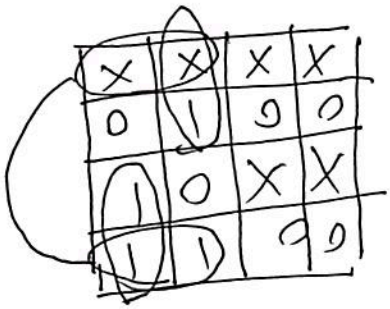


$D_A = Q_C X + Q_A \bar{Q}_C + Q_B \bar{Q}_C X$

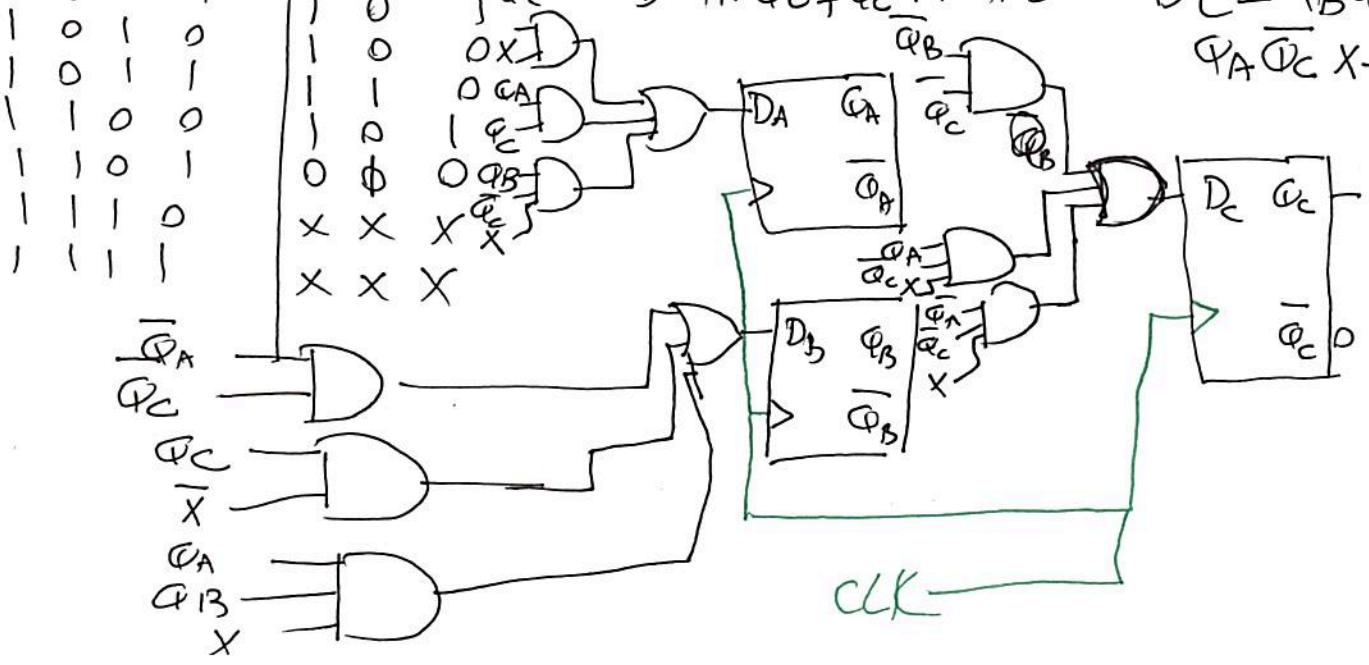
Q_A Q_B Q_C X	D_A D_B D_C (NS) Q_A Q_B Q_C
0 0 0 0	X
0 0 0 1	
0 0 1 0	
0 0 1 1	
0 1 0 0	1 1 0
0 1 0 1	0 ↑ 1
0 1 1 0	0 1 0
0 1 1 1	ϕ 0 0
1 0 0 0	0 1 1
1 0 0 1	1 0 1
1 0 1 0	1 0 0
1 0 1 1	0 ϕ 0
1 1 0 0	X X X
1 1 0 1	X X X
1 1 1 0	
1 1 1 1	



$D_B = \bar{Q}_A \bar{Q}_C + Q_C \bar{X} + Q_A Q_B X$



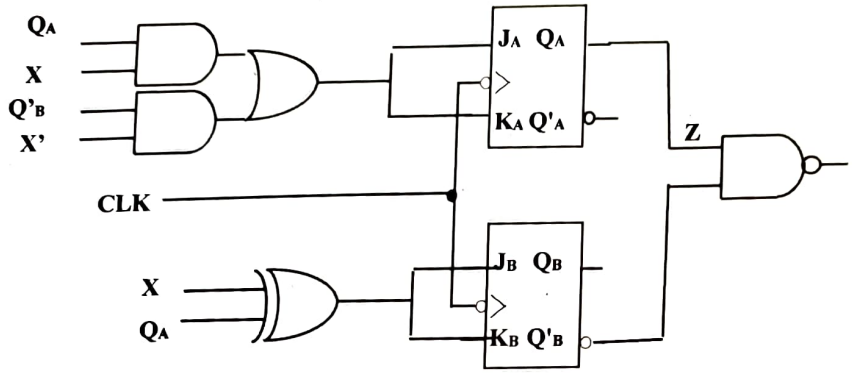
$D_C = \bar{Q}_B \bar{Q}_C + Q_A \bar{Q}_C X + Q_A \bar{Q}_C X$



EGC220 Quiz #19 Dr. Izadi

First NAME: key Last Name: _____

Analyze the following circuit leading to its state diagram.



1. $J_A = K_A = Q_A X + \overline{Q_B}\,\overline{X}$

$J_B = K_B = X \oplus Q_A$

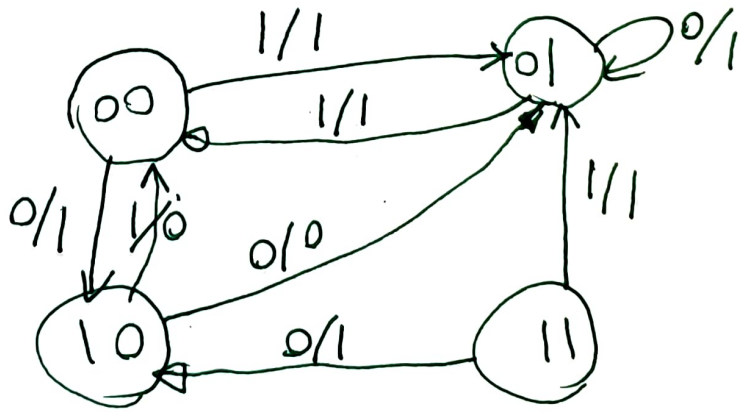
$Z = \overline{Q_A\,\overline{Q_B}} = \overline{Q_A} + Q_B$

2.

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

3.

Q_A	Q_B	X	$J_A=K_A$	$J_B=K_B$	$Q_A(t+1)$	$Q_B(t+1)$	Z
0	0	0	1	0	1	0	1
0	0	1	0	1	0	1	1
0	1	0	0	0	0	0	1
0	1	1	0	1	0	1	0
1	0	0	1	1	0	0	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	1	1
1	1	1	1	0			

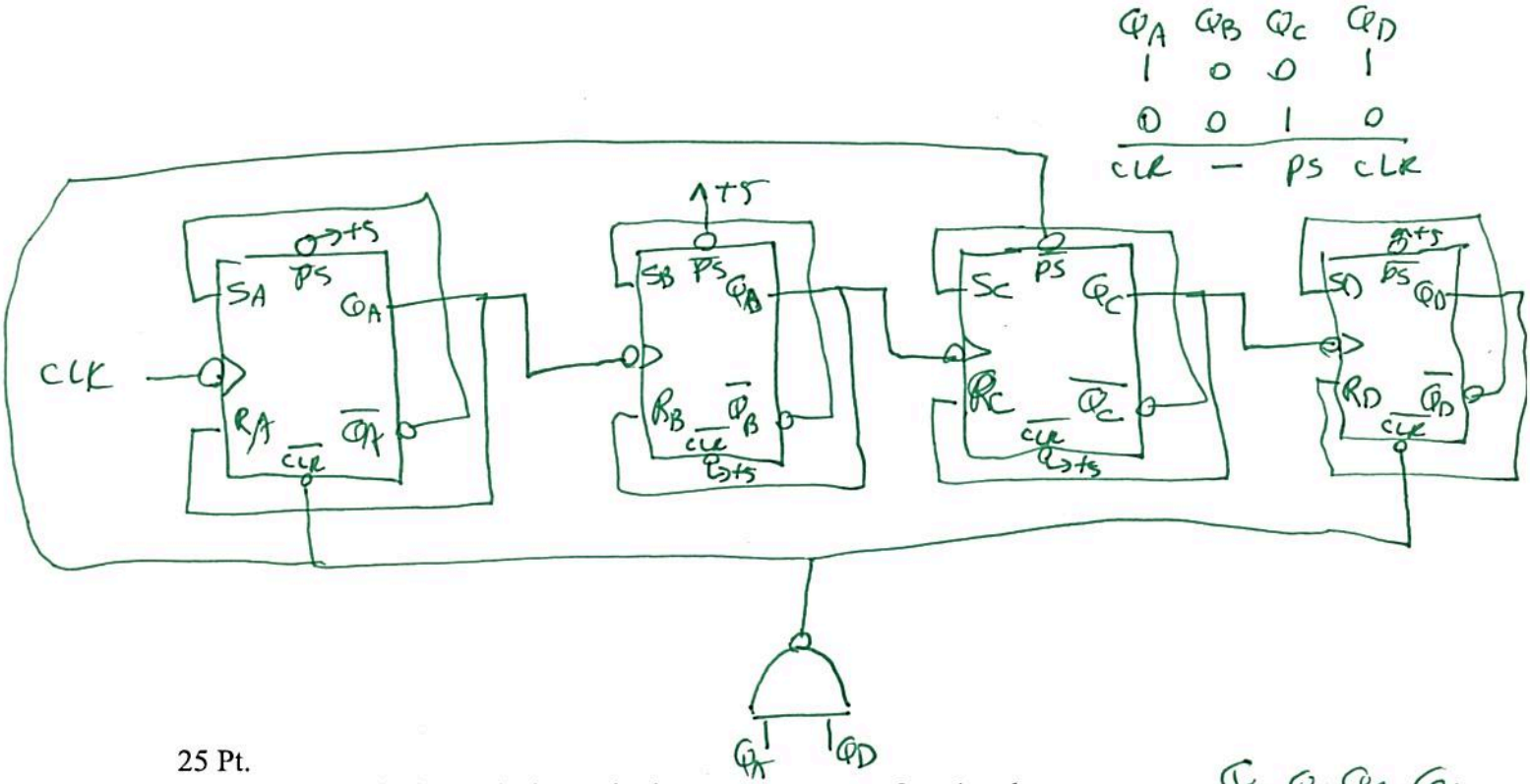


EGC220 Quiz #18 *Dr. Izadi*

First NAME:_____ Last Name:_____

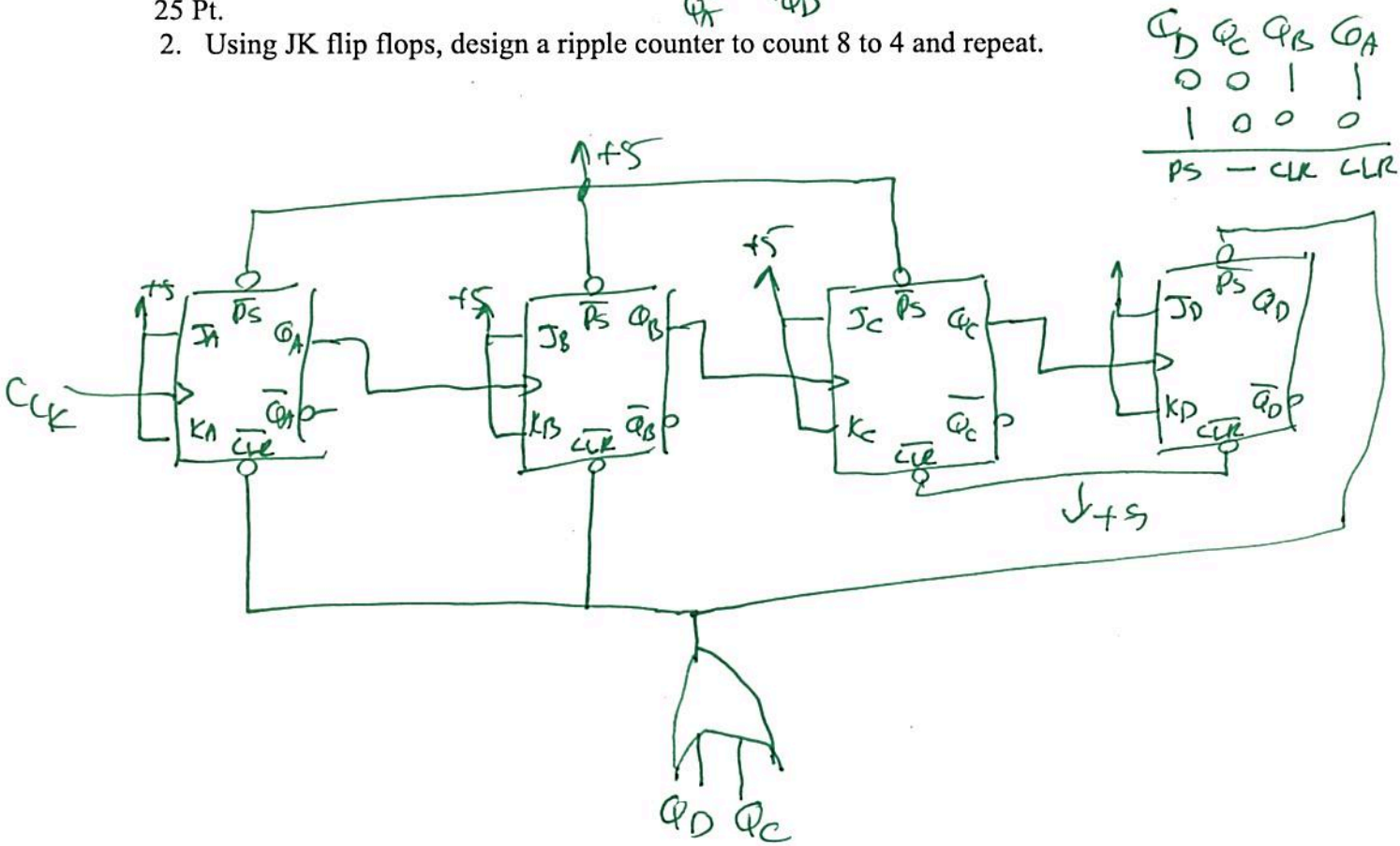
25 Pt.

1. Using SR flip flops, design a ripple counter to count from 4 to 8 and repeat.



25 Pt.

2. Using JK flip flops, design a ripple counter to count 8 to 4 and repeat.



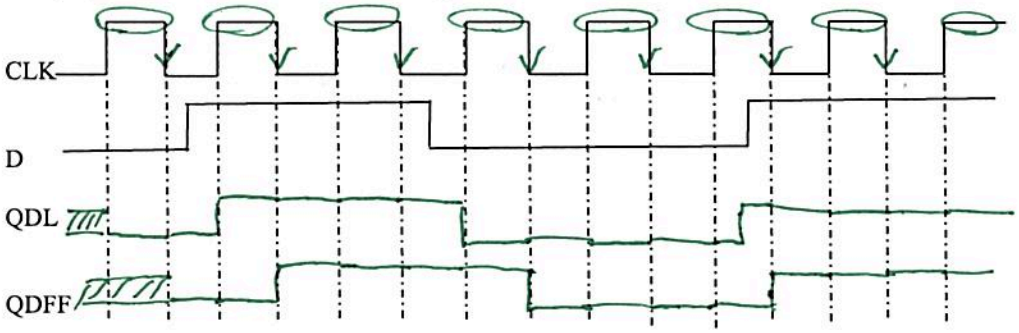
EGC220 Quiz #17 Dr. Izadi

First NAME:_____ Last Name:_____

15 PT.

Problem 1

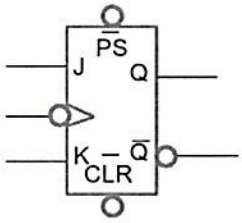
On the following graph, inputs CLK and *D* are shown. They are inputs to both a D latch and a D flip-flop. CLK goes into the **active high** G input ofthe D latch and **negative edge** clock input of the D flip-flop. Show the output of the D latch as *QDL* on the graph and the output of the D flip-flop as *QDFF* on the graph. Both outputs are initially 0 at the start of the graph, as shown. Do the two outputs differ, and if so, why?

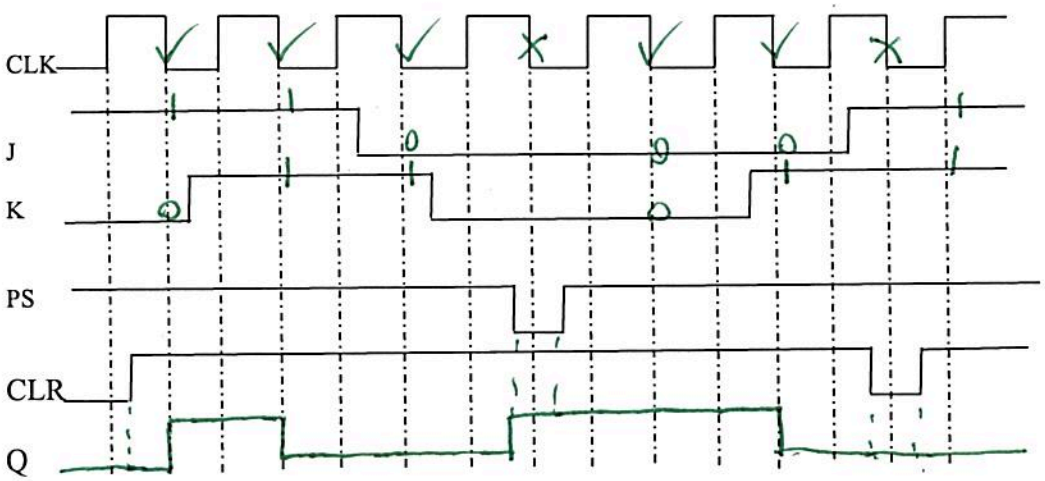


20 PT.

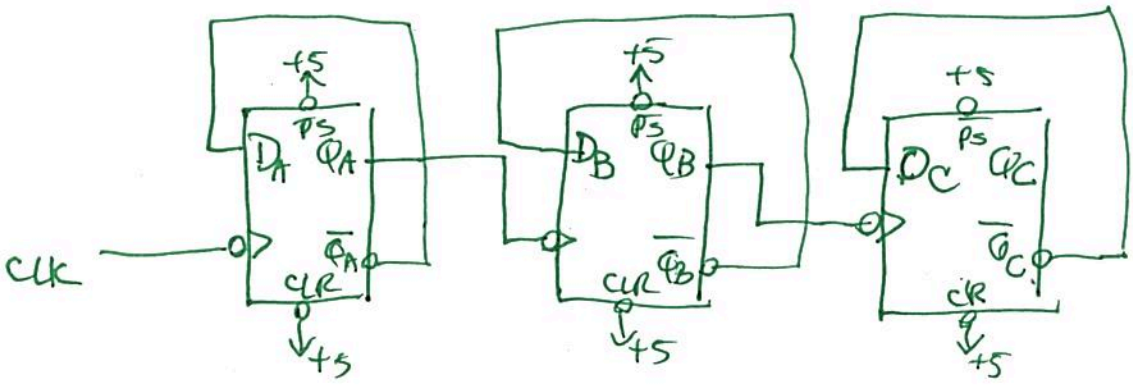
Problem 2

Complete the following timing diagram for a JK flip-flop with a low active preset (PS) and clear (CLR).





15 PT.
Problem 3
Using D flip-flops, design a ripple counter that counts 0 – 7 and repeats.

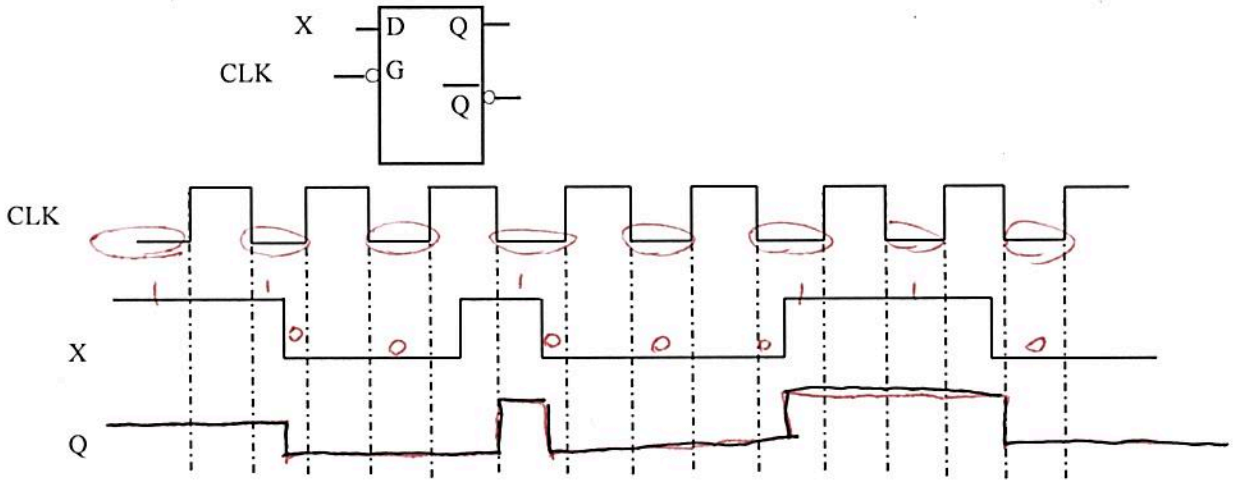


EGC220 Quiz #16 Dr. Izadi

First NAME: Key Last Name:_____

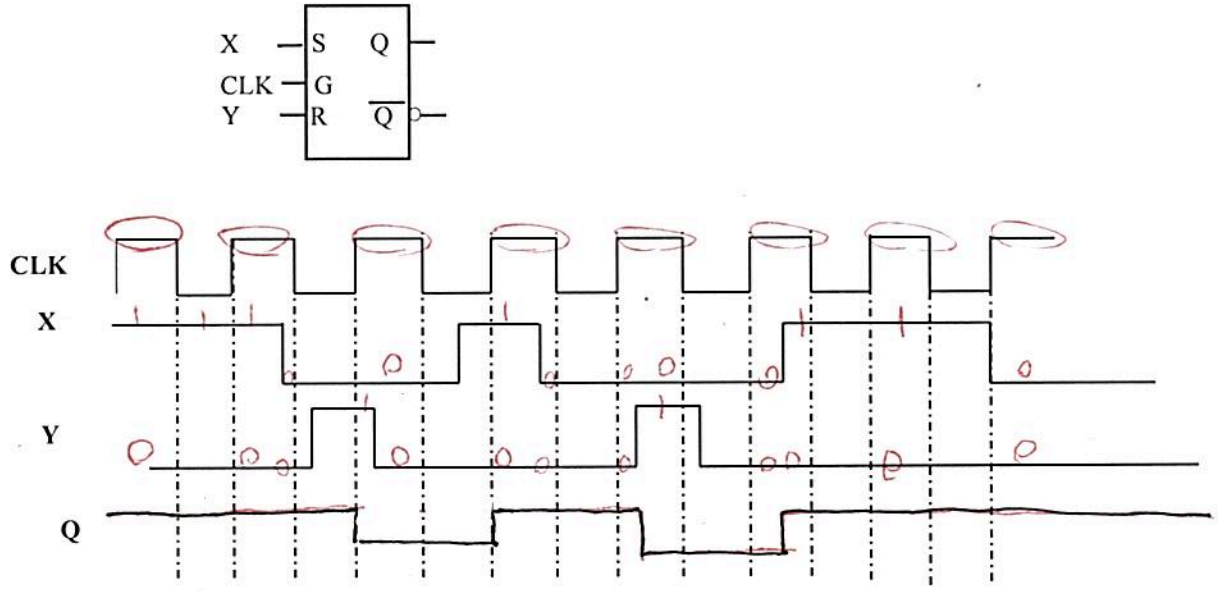
Problem 1 (25 PT.)

Complete the timing diagram if the following signals are applied as indicated.



Problem 2 (25 PT.)

Complete the timing diagram if the following signals are applied as indicated.



EGC220 Quiz #15 *Dr. Izadi*

First NAME:____Key_____ Last Name_____

25 Points

Using dataflow aspect of Verilog, design a 1 – out of 8 decoder, with one high active enable line E. The code is partially written.

```
module decoder (A,B, C,E, D0,D1,D2,D3, D4, D5, D6, D7);
input  A,B,C, E ;
output  D0,D1,D2,D3, D4,D5,D6,D7;
assign  D0 = ~A&~B&~C&E;
assign  D1 = ~A&~B&C&E;
assign  D2 = ~A&B&~C &E;
assign  D3 =~ A&B&C &E;
assign  D4 = A&~B&~C&E
assign  D5 = A&~B&C&E;
assign  D6 = A&B&~C &E;
assign  D7 = A&B&C &E;
endmodule
```

25 Points

Problem 2

Using Verilog, design a 4× 1 Mux. The code is partially written. You have the choice of Dataflow or Behavioral

Behavioral

```
module Mux (S1, S0,,I0,I1,I2,I3,Y);
input S1, S0;
input I0,I1,I2,I3;                                  ;
output   Y;                                  ;
reg  Y;
always @ (S1, S0, , I0,I1,I2,I3)
if (~S1&~S0) Y = I0;
else if (~S1&S0), Y = I1;
else if ((S1&~S0) Y = I2;
else Y=I3;
endmodule
```

Dataflow

```
module Mux (S1, S0,I0,I1,I2,I3, Y);
input  S1, S0;
input I0,I1,I2,I3;                                  ;
output   Y;                                  ;
assign Y = ~S1&~S0&I0 | ~S1&S0&I1 | S1&~S0&I2 | S1&S0&I3;
endmodule
```

EGC220 Quiz #15 *Dr. Izadi*

First NAME:____Key_____ Last Name_____

25 Points

Using dataflow aspect of Verilog, design a 1 – out of 8 decoder, with one high active enable line E. The code is partially written.

```
module decoder (A,B, C,E, D0,D1,D2,D3, D4, D5, D6, D7);
input  A,B,C, E ;
output  D0,D1,D2,D3, D4,D5,D6,D7;
assign  D0 = ~A&~B&~C&E;
assign  D1 = ~A&~B&C&E;
assign  D2 = ~A&B&~C &E;
assign  D3 =~ A&B&C &E;
assign  D4 = A&~B&~C&E
assign  D5 = A&~B&C&E;
assign  D6 = A&B&~C &E;
assign  D7 = A&B&C &E;
endmodule
```

25 Points

Problem 2

Using Verilog, design a 4× 1 Mux. The code is partially written. You have the choice of Dataflow or Behavioral

Behavioral

```
module Mux (S,I0,I1,I2,I3,Y);
input [1:0] S;
input I0,I1,I2,I3;                                  ;
output   Y;                                  ;
reg  Y;
always @ (S, I0,I1,I2,I3)
if (S==0) Y = I0;
else if (S==1) Y = I1;
else if (S==2) Y = I2;
else Y=I3;
endmodule
```

Dataflow

```
module Mux (S,I0,I1,I2,I3, Y);
input [1:0] S;
input I0,I1,I2,I3;                                  ;
output   Y;                                  ;
assign Y = ~S(1)&~S(0)&I0 | ~S(1)&S(0)&I1 | S(1)&~S(0)&I2 |
S(1)&S(0)&I3;
endmodule
```

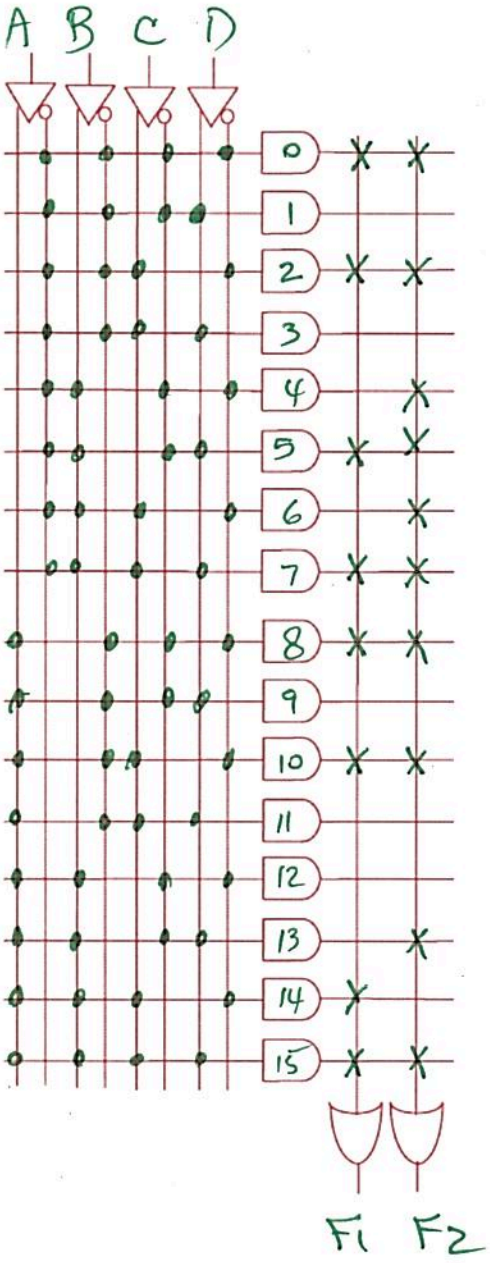
EGC220 Quiz #14 *Dr. Izadi*

First NAME: Key Last Name:_____

15 PT.

1. Implement the following functions using a PLE. Mark fixed and programmable cross points by ▪ and ×, respectively.

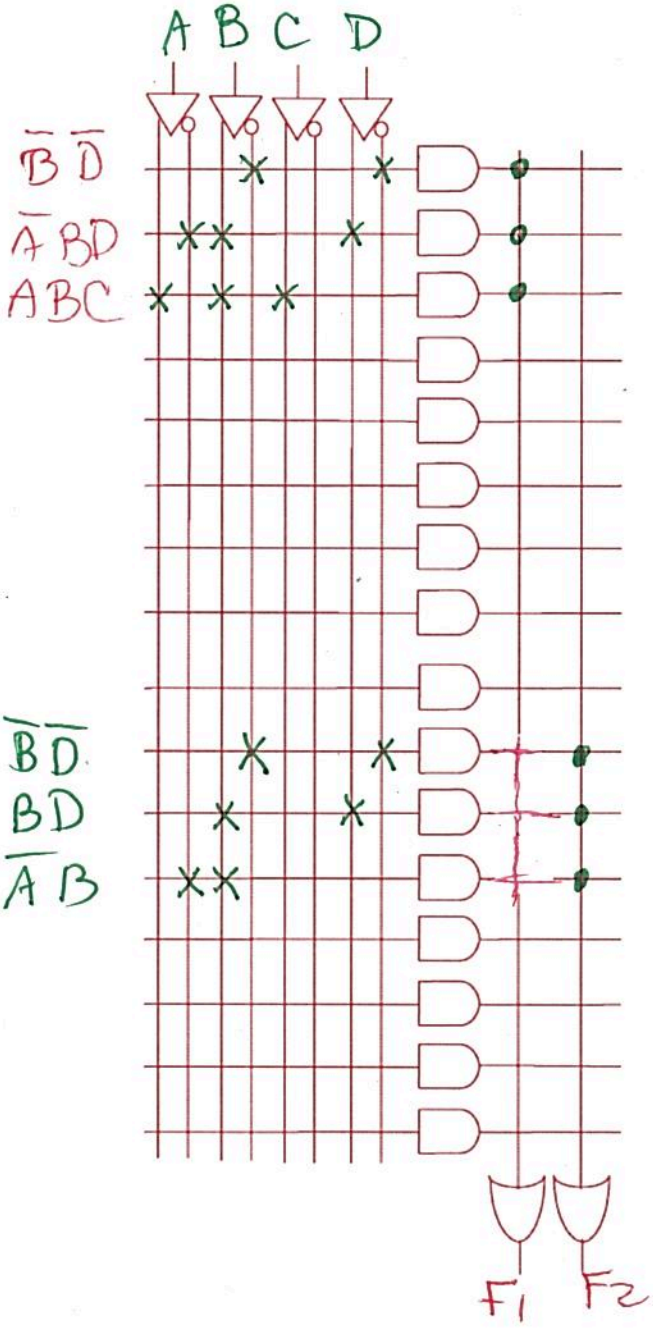
   $F_1 = \sum m\,(0,2,5,7,8,10,14,15)$
   $F_2 = \sum m\,(0,2,4,5,6,7,8,10,13,15)$

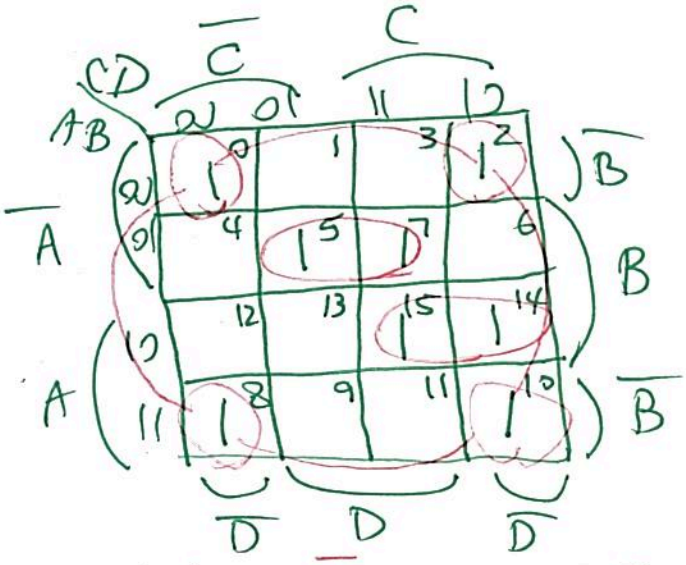


15 PT.

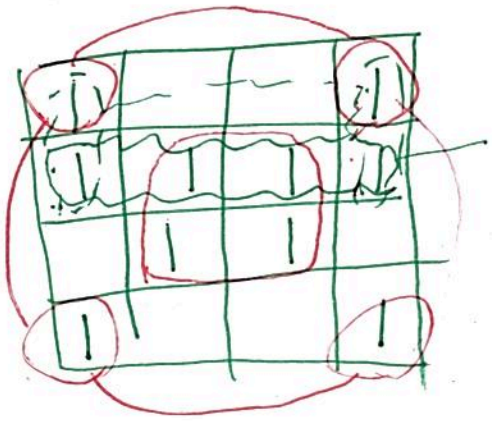
2. Implement the following functions using a PAL. Mark fixed and programmable cross points by ▪ and ×, respectively.

$F_1 = \sum m\ (0,2,5,7,8,10,14,15)$
$F_2 = \sum m\ (0,2,4,5,6,7,8,10,13,15)$





$F_1 = \bar{B}\bar{D} + A\bar{B}D + AB\bar{C}$

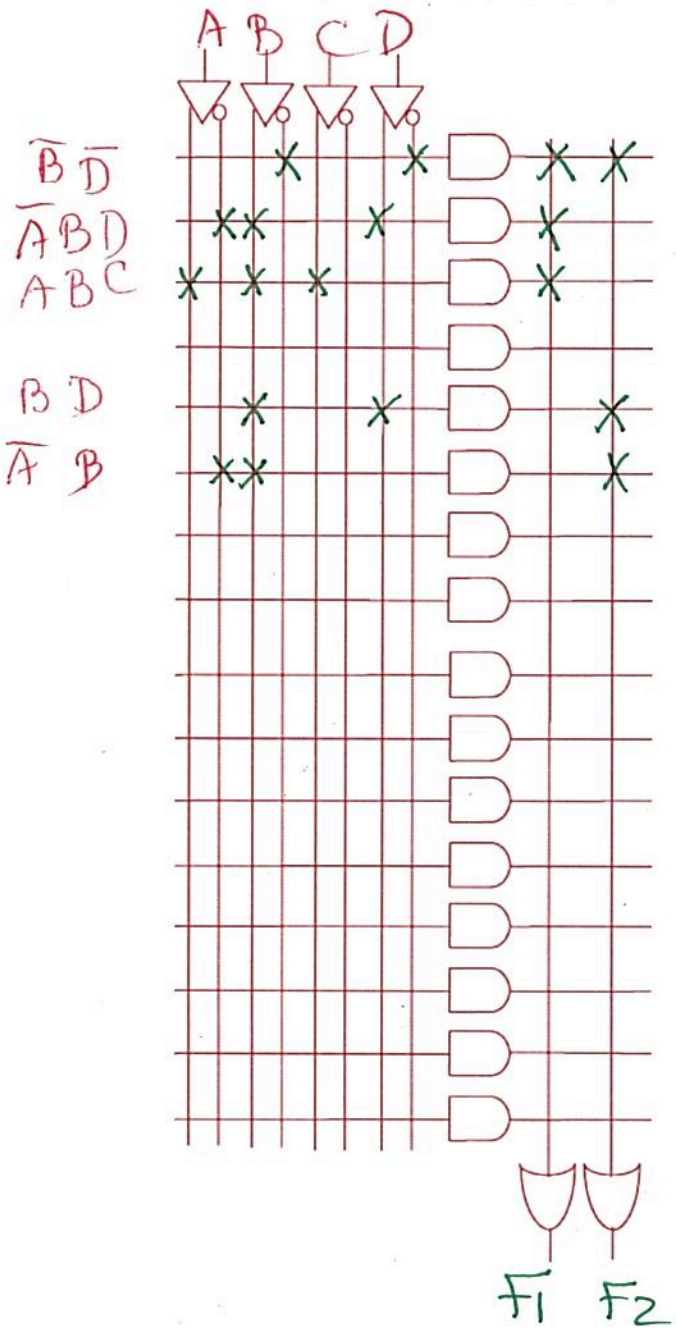


$F_2 = \bar{B}\bar{D} + BD + \bar{A}B$
or
$\bar{A}\bar{D}$

20 PT.

3. Implement the following functions using a PLA. Mark fixed and programmable cross points by ▪ and ×, respectively.

$F_1 = \sum m\,(0,2,5,7,8,10,14,15)$
$F_2 = \sum m\,(0,2,4,5,6,7,8,10,13,15)$



EGC220 Key Quiz #13 *Dr. Izadi*

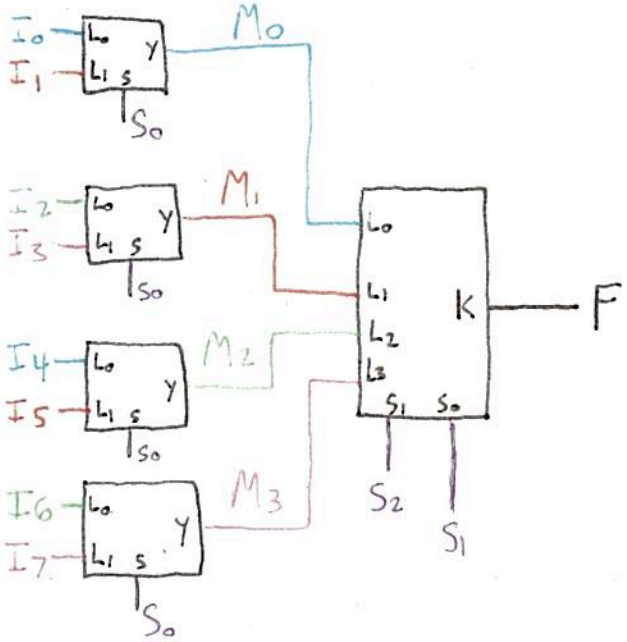
First NAME:_____ Last Name:_____ _____

Problem 1

Implement an 8 × 1 Mux using four 2 × 1 Mux's and one 4 × 1 Mux.

S_2	S_1	S_0	F	
0	0	0	I_0	M_0
0	0	1	I_1	
0	1	0	I_2	M_1
0	1	1	I_3	
1	0	0	I_4	M_2
1	0	1	I_5	
1	1	0	I_6	M_3
1	1	1	I_7	

K



Problem 2

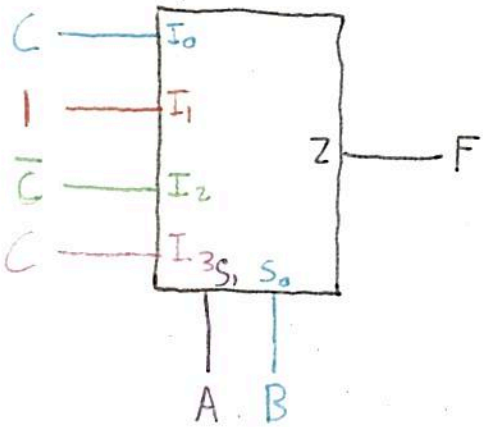
Implement the following function using a 4 × 1 Mux.

$F(A, B, C) = \sum m\ (1, 2. 3. 4, 7)$

A B

S_1	S_0	Z
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

A	B	C	F	
0	0	0	0	C
0	0	1	1	
0	1	0	1	1
0	1	1	1	
1	0	0	1	$\bar{C}$
1	0	1	0	
1	1	0	0	C
1	1	1	1	

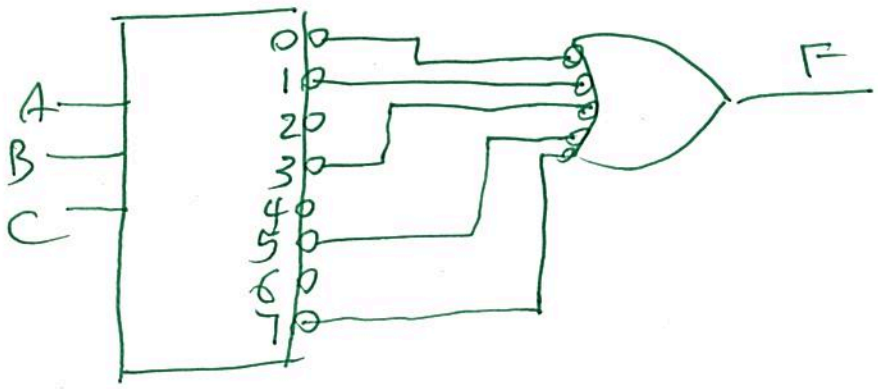


EGC220 Quiz #12 Dr. Izadi

First NAME: Key Last Name: _____

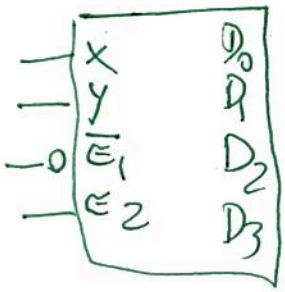
25 PT.

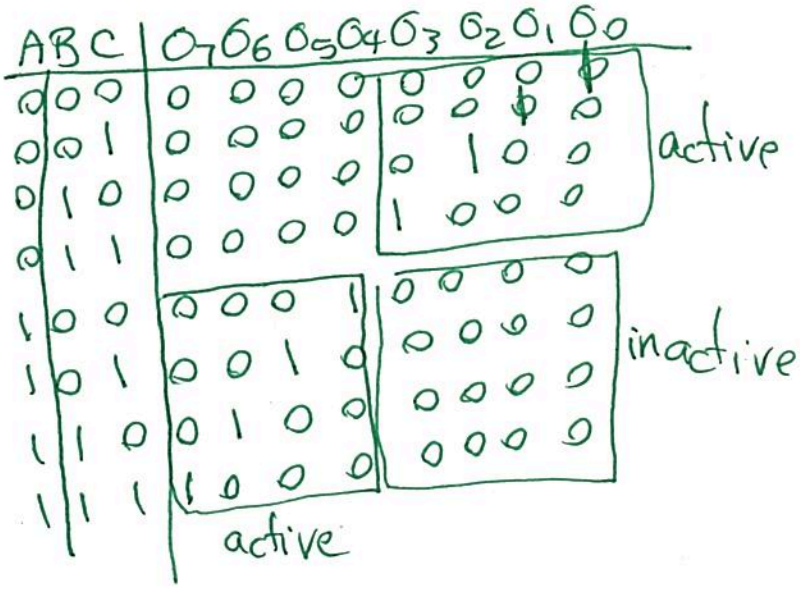
1. Implement the following Boolean expression using a decoder and a NAND gate.
   $F(A,B,C) = \sum m\,(0, 1, 3, 5, 7) + d(4, 6)$

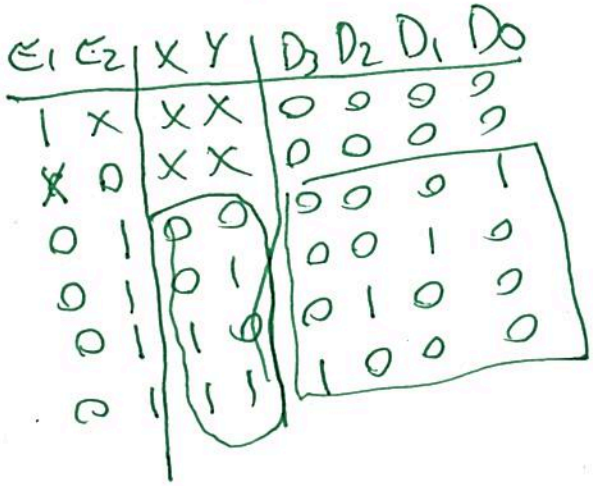


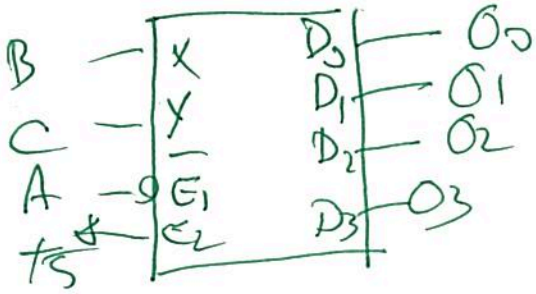
25 PT.

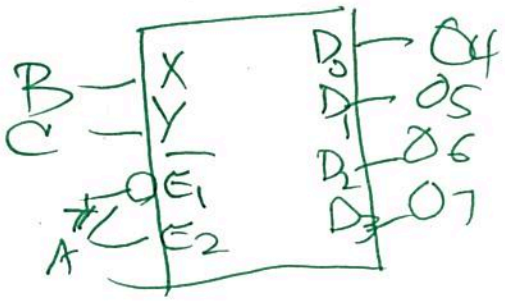
2. Design a 1-out-of 8 decoder with high active outputs, using 1-out-of 4 decoder with two active low enable lines and one active high enable line.











EGC220 Quiz #11 Dr. Izadi

First NAME: Key Last Name: _____

30 Points

1. Design a 1-out-of 8 decoder with active low outputs, three enable inputs: E1 and E2 (high active), and E3 (low active). You need to show a block diagram, set of equations, and the logic implementation.

E_1	E_2	$\bar{E}_3$	A	B	C	$\bar{O}_7$	$\bar{O}_6$	$\bar{O}_5$	$\bar{O}_4$	$\bar{O}_3$	$\bar{O}_2$	$\bar{O}_1$	$\bar{O}_0$
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	0	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	1	0	0	0	0	1	1	1	1	1	1	1	0
1	1	0	0	0	1	1	1	1	1	1	1	0	1
1	1	0	0	1	0	1	1	1	1	1	0	1	1
1	1	0	0	1	1	1	1	1	1	0	1	1	1
1	1	0	1	0	0	1	1	1	0	1	1	1	1
1	1	0	1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	1	0	1	0	1	1	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1	1	1	1

$\bar{O}_0 = E_1 E_2 \bar{E}_3 \bar{A} \bar{B} \bar{C}$

$\bar{O}_1 = E_1 E_2 \bar{E}_3 \bar{A} \bar{B} C$

$\bar{O}_2 = E_1 E_2 \bar{E}_3 \bar{A} B \bar{C}$

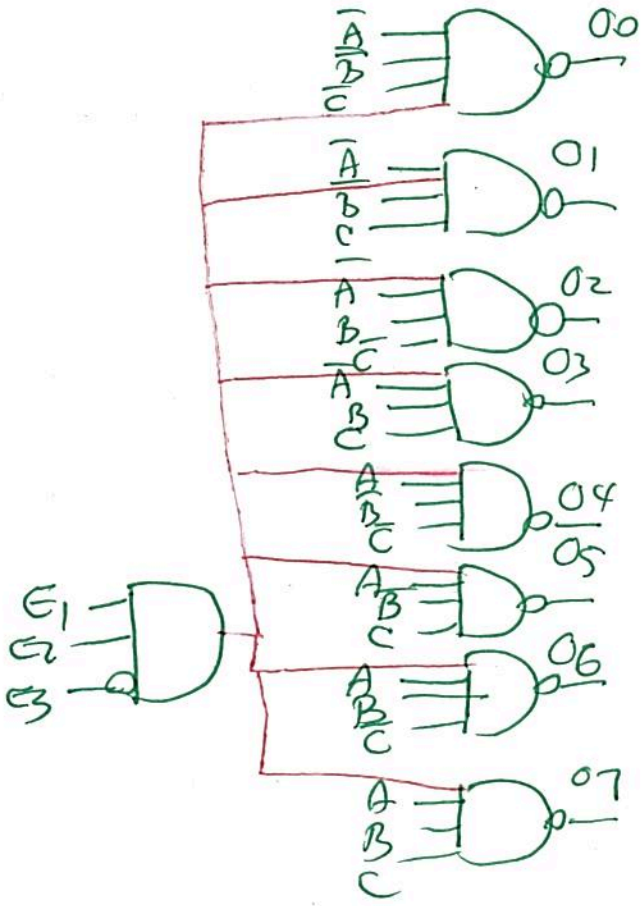
$\bar{O}_3 = E_1 E_2 \bar{E}_3 \bar{A} B C$

$\bar{O}_4 = E_1 E_2 \bar{E}_3 A \bar{B} \bar{C}$

$\bar{O}_5 = E_1 E_2 \bar{E}_3 A \bar{B} C$

$\bar{O}_6 = E_1 E_2 \bar{E}_3 A B \bar{C}$

$\bar{O}_7 = E_1 E_2 \bar{E}_3 A B C$



20 Points

2. Show the truth table only of a circuit that converts a 4-bit Gray code to its equivalent 4-bit BCD code.

BCD	GRAY
0	0 0 0 0
1	0 0 0 1
2	0 0 1 1
3	0 0 1 0
4	0 1 1 0
5	0 1 1 1
6	0 1 0 1
7	0 1 0 0
8	1 1 0 0
9	1 0 1
	x 1 1 1 1
	x 1 1 1 0
	x 1 0 1 0
	x 1 0 1 1
	x 1 0 0 1
	x 1 0 0 0

GREY	A B C D
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 0	0 0 1 1
0 0 1 1	0 0 1 0
0 1 0 0	0 1 1 1
0 1 0 1	0 1 1 0
0 1 1 0	0 1 0 0
0 1 1 1	0 1 0 1
1 0 0 0	x x x x
1 0 0 1	x x x x
1 0 1 0	x x x x
1 0 1 1	x x x x
1 1 0 0	1 0 0 0
1 1 0 1	1 0 0 1
1 1 1 0	x x x x
1 1 1 1	x x x x

EGC220 Quiz #10 Dr. Izadi

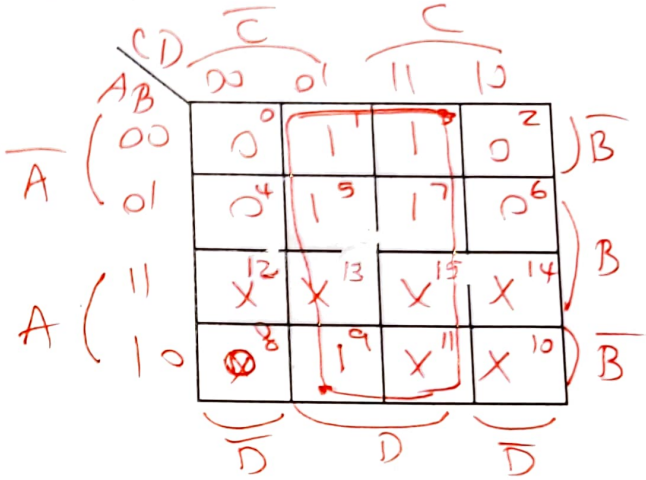
First NAME: key Last Name: _____

Design a circuit that has 4 inputs, labeled A, B, C and D, and one output F. The output is 1 if and only if the BCD input combination is an odd decimal number i.e. 0101 represents 5 which is an odd decimal number and 0100 represents 4, which is not odd.
Note; Non-BCD input combinations would not be entered.

a. (20 Pt.) Write the truth table for this circuit.
b. (20 Pt.) Find the minimized logic equations in SOP for the output
c. (10 Pt.) Draw the corresponding all NAND gates logic diagram for this circuit. Label all inputs and outputs.

a

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X



b.

$F = D$

EGC220 Quiz #9 Dr. Izadi

First NAME:_____ Last Name:_____

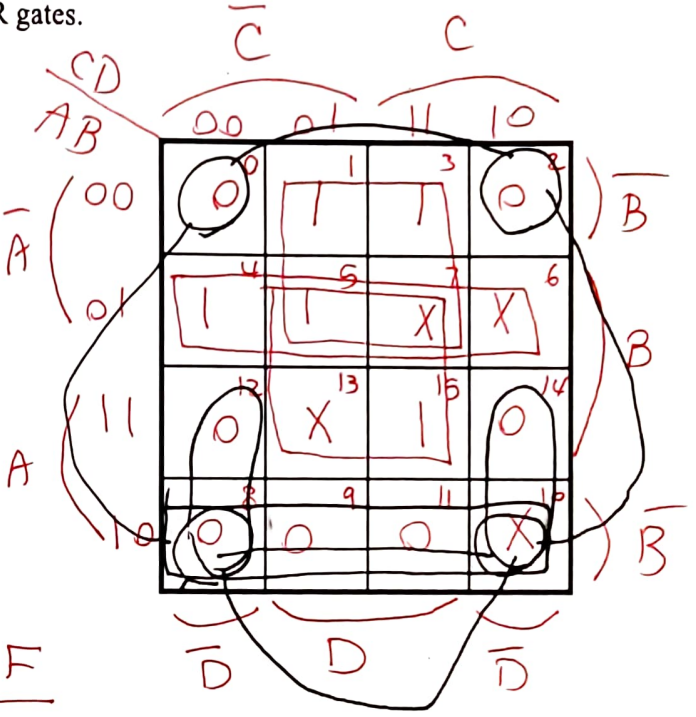
For Boolean expression F(A, B, C, D) = ∑m(1, 3, 4, 5, 15)+ d(6, 7, 10, 13), determine

a. Minimum sum of products.
b. Minimum products of sums.
c. Gate implementation using all NAND gates.
d. Gate implementation using all NOR gates.

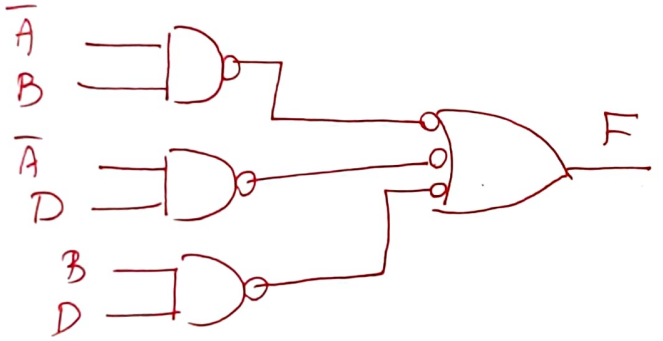
① $F = \bar{A}B + \bar{A}D + BD$

② $\bar{F} = A\bar{B} + A\bar{D} + \bar{B}\bar{D}$

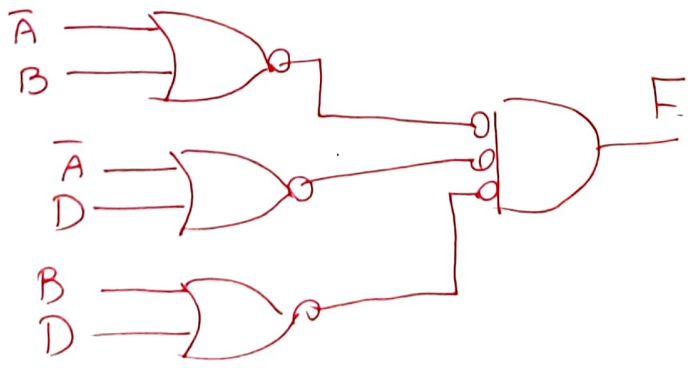
$F = (\bar{A}+B)(\bar{A}+D)(B+D)$



C)



D)



EGC220 Quiz #8 Dr. Izadi

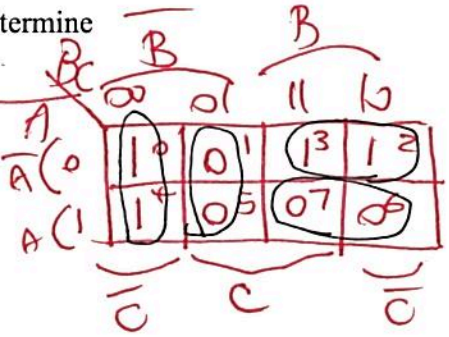
First NAME: Key Last Name: _____

For the following Boolean expression F(A,B,C) = ∑m(0, 2, 3, 4), determine

a. Truth table.
b. Sum of min terms.
c. Product of max terms.
d. Standard sum of products.
e. Standard product of sums.
f. Minimum sum of products using a K-map.
g. Minimum products of sums using a K-map.
h. Gate implementation using all NAND gates.
i. Gate implementation using all NOR gates.
j. Use the Boolean identities to get the answer in part f.

a.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



b. $F = \sum m(0, 2, 3, 4)$

c. $F = \Pi M(1, 5, 6, 7)$

d. $F = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$

e. $\bar{F} = \bar{A}\bar{B}C + A\bar{B}C + AB\bar{C} + ABC$

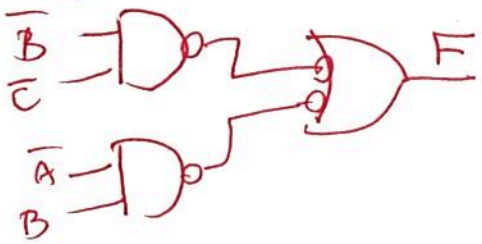
$F = (A+B+\bar{C})(\bar{A}+B+\bar{C})(\bar{A}+\bar{B}+C)(\bar{A}+\bar{B}+\bar{C})$

f. $F = \bar{B}\bar{C} + \bar{A}B$

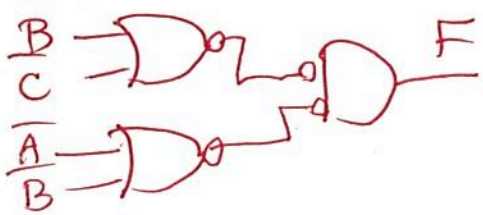
g. $\bar{F} = \bar{B}C + AB$

$F = (B+\bar{C})(\bar{A}+\bar{B})$

h.



i.



j.

$F = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C$

$= \bar{B}\bar{C}(\bar{A}+A) + \bar{A}B(\bar{C}+C)$

$= \bar{B}\bar{C} + \bar{A}B$

EGC220 Quiz #7 Dr. *Izadi*

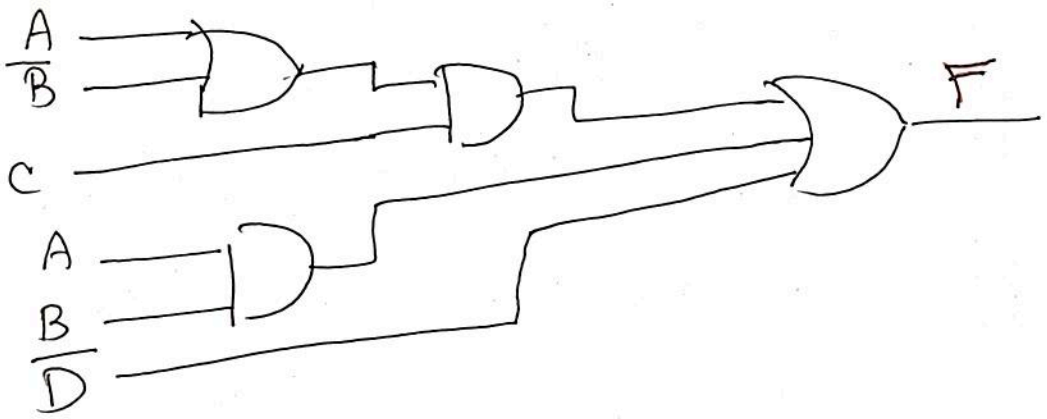
First NAME: Key Last Name: _____

25 PT.

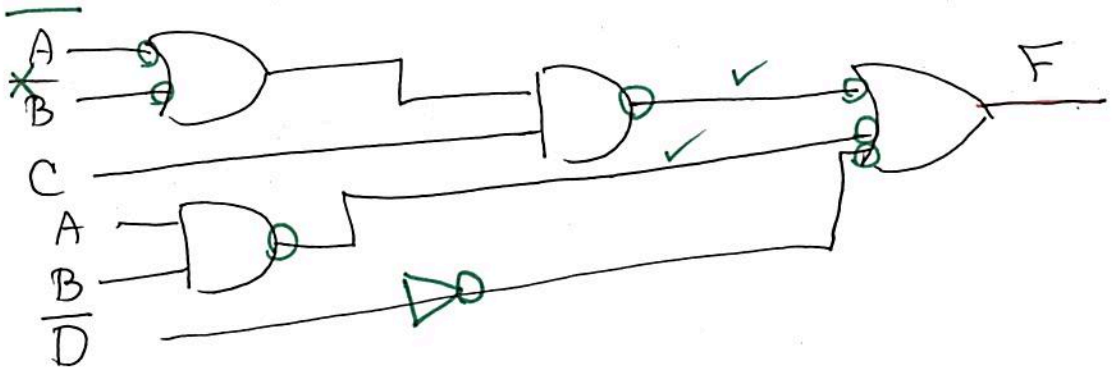
1.

a. Draw the logic diagrams for F = (A+B')C + AB+ D' using AND, OR and NOT gates without altering the expression in any way.
b. Convert the circuit in part a. to NAND gates.
c. Convert the circuit in part a. to all NOR gates.

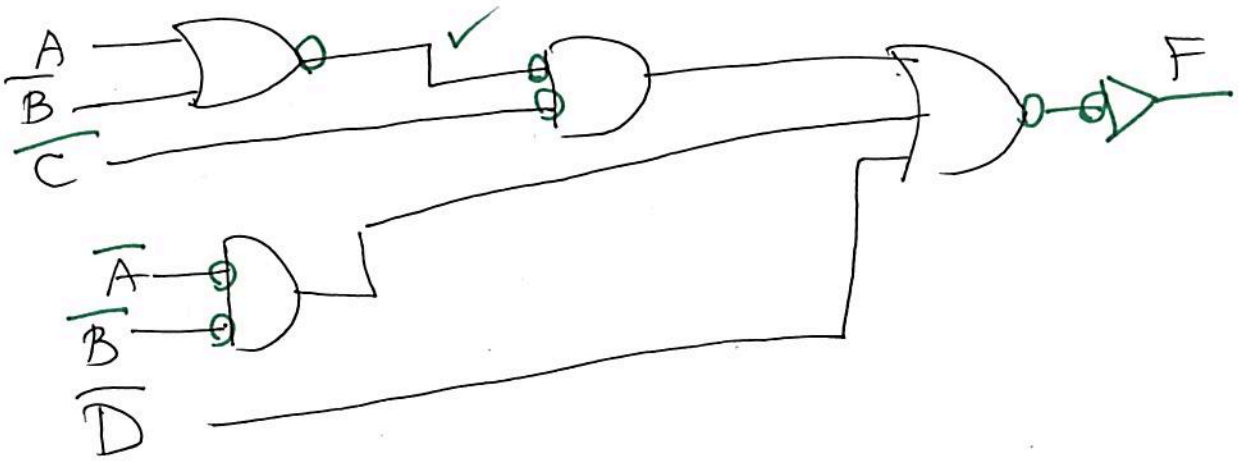
a.



b



c.



25 PT.

2. For the following Boolean expression F = A'B' + B'C + BC', determine
   a. truth table
   b. Sum of min terms
   c. Product of max terms
   d. Standard sum of products
   e. Standard product of sums
   f. Minimum sum of products

a.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

b. $F = \Sigma m(0,1,2,5,6)$

c. $F = \Pi M(3,4,7)$

d. $F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + AB\bar{C}$

e. $\bar{F} = \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$

$F = (A+\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+\bar{B}+\bar{C})$

f. $F = \bar{A}B(C+\bar{C}) + \bar{B}C(\bar{A}+A) + B\bar{C}(\bar{A}+A)$

$= \bar{A}\bar{B} + \bar{B}C + B\bar{C}$

EGC220 Quiz #6 Dr. *Izadi*

First NAME:_____ Last Name:_____

10 PT.

1. Find the dual of F = A'(D'+C'D) + B(A + A'CD)

$$(\bar{A} + (\bar{D}(\bar{C}+D)))(B + A(\bar{A}+C+D))$$

10 PT.

2. Find the complement of $\overline{F} = \overline{A'(D'+C'D) + B(A + A'CD)}$

$$\overline{F} = \overline{(\bar{A}(\bar{D}+\bar{C}D))} \cdot \overline{(B(A+\bar{A}CD))}$$
$$= (A + \overline{(\bar{D}+\bar{C}D)})(\bar{B} + \overline{(A+\bar{A}CD)})$$
$$= (A + D(C+\bar{D}))(\bar{B} + (\bar{A}(A+\bar{C}+\bar{D})))$$

15 PT.

16 Given $Y(A, B, C) = \Pi M(0, 1, 4, 7)$, write the complete truth table for $G = \overline{Y} = \Sigma m(0,1,4,7)$

A B C	G
0 0 0	1
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	1

15 PT.

16 Simplify the following expression using the postulates and theorems of Boolean algebra. Eliminate all group complements. Justify each step by stating or referring to the Boolean theorem or postulate you use. Don't skip any steps!

$F(A, B, C) = \sum m(0, 1,4, 6)$

$$F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + AB\bar{C}$$

(14) (14)

$$= \bar{A}\bar{B}(\bar{C}+C) + A\bar{C}(\bar{B}+B)$$

(7) (7)

(2) (2)

$$= \bar{A}\bar{B} + A\bar{C}$$

EGC220 Quiz #5 Dr. Izadi

First NAME: Key Last Name: _____

Note: B' = $\underline{B}$

A	B	$\overline{A \oplus B}$	$\bar{A} \oplus B$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

5 PT.

1. Indicate the following property is T (true) or F (False)

(T) F $\bar{A} \oplus B = \overline{A \oplus B}$

$A \oplus B = \bar{A}B + A\bar{B}$ $\bar{A} \oplus B = AB + \bar{A}\bar{B}$

$\overline{A \oplus B} = \bar{A}\bar{B} + AB$

5 PT.

2. Indicate the following property is T (true) or F (False)

(T) F $A'BC' + A'BC + AB' = A \oplus B$

$\bar{A}B(\bar{C}+C) + A\bar{B}$

$\bar{A}B + A\bar{B} = A \oplus B$

5 PT.

3. Which of the following is the dual of AB'+D'
   a. (A+B)' D
   b. (A+B')D'
   c. A + B'D
   d. (A'+B)D
   e. None of the above

5 PT.

4. Which of the following is the complement of AB'+D'
   a. (A+B)' D
   b. (A+B')D
   c. A + B'D
   d. (A'+B)D'
   e. None of the above

$\overline{A\bar{B} + \bar{D}} = \overline{(A\bar{B})}\,\bar{\bar{D}}$

$= (\bar{A} + B)D$

5 PT

5. Mark all which is true
   a. $\bar{A}B + A\bar{B} = 1$
   b. $AB + \bar{A}\bar{B} = 1$
   c. $AB + \overline{A\,B} = 1$
   d. $A \oplus \bar{B} = 1$
   e. None of the above

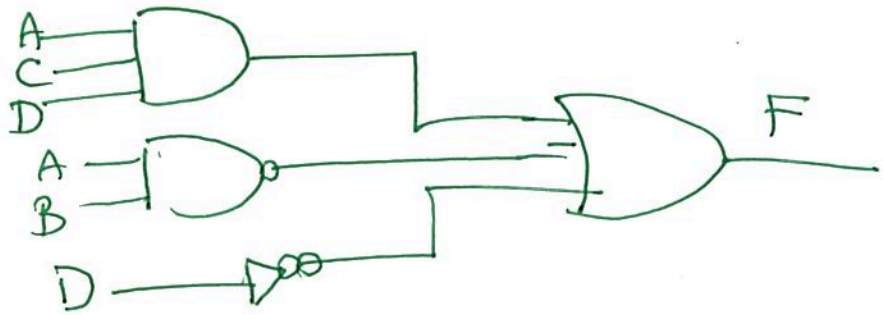
9 PT.

6. By means of a truth table prove or disprove that (A+B')C = B'C + AC

A	B	C	A+B̄	(A+B̄)C	B̄C + AC
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	1	1

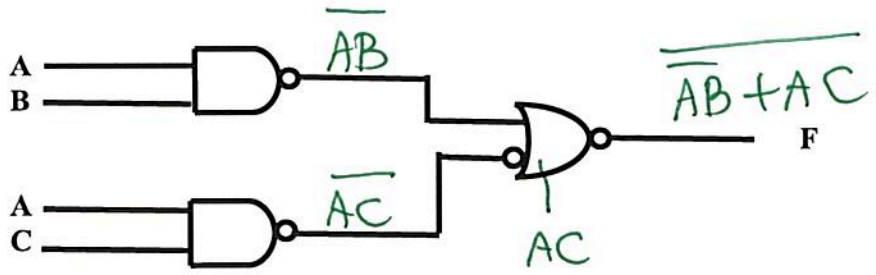
8 PT.

7. Using AND, OR, and NOT gates, draw the logic diagrams for Boolean expression F=ACD + (AB)' + D' without expanding or simplifying.



8 PT.

8. Write the Boolean expression of following logic diagram. Don't simplify.



EGC220 **Quiz #4** Dr. *Izadi*

First NAME: Key **Last Name:**_____

10 PT.

1. Complete the following table of equivalent values. Use 8 bit binary number i.e. xxxxxxx.x

Decimal	Unsigned	Signed Magnitude	Singed 2's complements
24.5	0011 000.1	0011 000.1	0011 000.1
-24.5	X	1 011 000.1	1 1 0 0 1 1 1.1

S 32 16 8 4 2 1, .5

10 PT.

2. Perform the following operations in binary. Assume signed 2's complement notation.
   a. 48 + 22

64	32	16	8	4	2	1	
0	0	1	1	0	0	0	+48
0	0	0	1	0	1	0	+22
0	1	0	0	0	1	0	+70

   b. 48 – 22

	128	64	32	16	8	4	2	1
-22	1	1	1	0	1	0	1	0
+48	0	0	1	1	0	0	0	0
+26	0	0	0	1	1	0	1	0

CY = 1

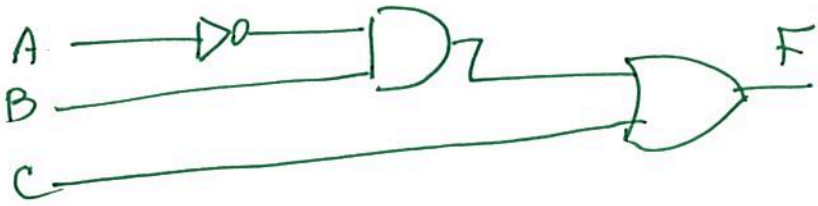
10 PT.

3. Find the truth table for $F = A\,B + \overline{C}$

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

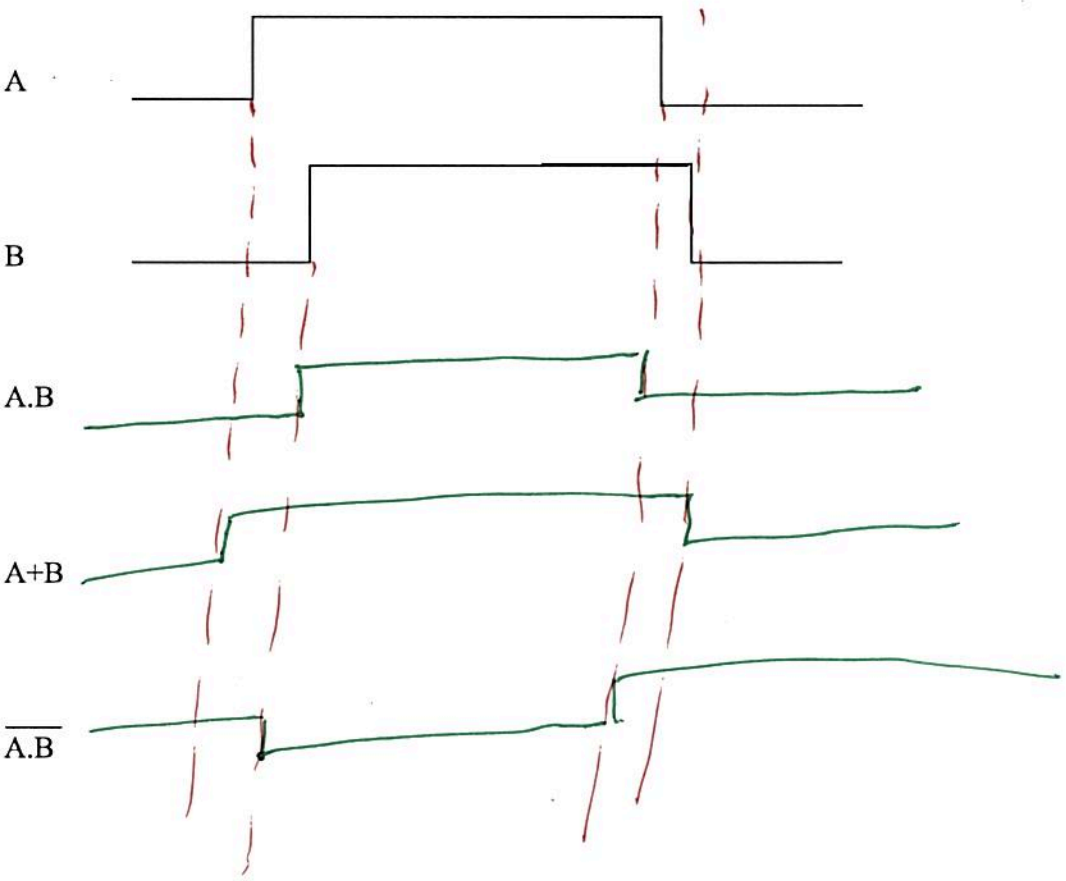
10 PT.

4. Draw a logic diagram for $F = \overline{A}\,B + C$ using AND, OR, and NOT gates.



10 PT.

5. Complete the time diagram for the following gate



EGC220 **Quiz #3** *Dr. Izadi*

First NAME: Key **Last Name:**_____

Problems 1 – 6 (5 pt. each) 7 (20 pt. each)

1. Which of the following is 9th complement of decimal numbers 87097

   99999
   12902

   a. 12901
   b. 12902
   c. 12903
   d. None of the above

2. Which of the following is 10th complement of decimal numbers 87097
   a. 12901
   b. 12902
   c. 12903
   d. None of the above

3. Which of the following is 16th complement of $(CF3.B)_{16}$

   FFFF
   30C.4 → 15th Comp
   1
   30C.5 → 16th Comp

   a. 41D.5
   b. 0C.4
   c. 34D.B
   d. 34C.B
   e. None of the above

8421

4. What does 1010_2 represent in unsigned domain
   a. 10_{10}
   b. -2_{10}
   c. 12_{10}
   d. -6_{10}
   e. None of the above

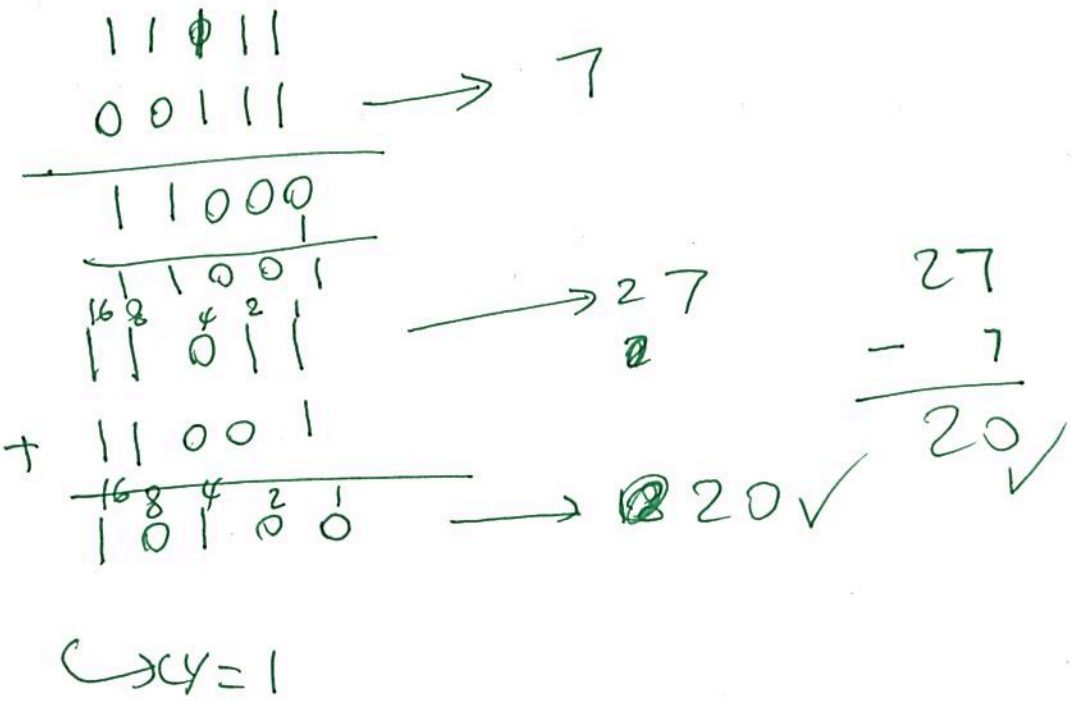
5. What does 1010 represent in signed magnitude domain
   a. 10_{10}
   b. -2_{10}
   c. 12_{10}
   d. -6_{10}
   e. None of the above

6. What does 1010 represent in signed 2's complement domain

   − 0110

   a. 10_{10}
   b. -2_{10}
   c. 12_{10}
   d. -6_{10}
   e. None of the above 11_{10}

7. Perform subtraction on the following unsigned binary numbers using the 2's complement of the subtrahend. If the result should be negative, 2's complement it and affix a minus sign.
You need to show detailed work.
11011 – 0111



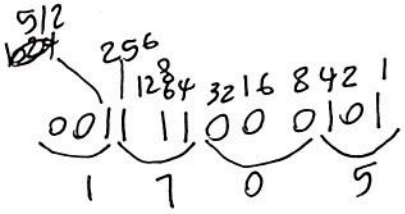
EGC220 **Quiz #2** *Dr. Izadi*

First NAME:_____ **Last Name:**_____

Problems 1 – 3 mark all that is correct

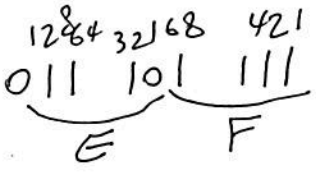
5 PT. 8421

1) Binary 1101 is equivalent to
   a. 14 in base 10
   b. D in base 16
   c. 15 in base 8
   d. Is not a valid binary number



5 PT.

2) Hexadecimal 3C5 is equivalent to
   a. 1987 in base 10
   b. 001111000101 in base 2
   c. 1705 in Octal
   d. Is not a valid number



5 PT.

3) Octal 357 is equivalent to
   a. 359 in decimal
   b. EF in Hexadecimal
   c. 11101111 in binary
   d. Is not a valid number

10 PT.

4) Perform the following arithmetic operation in the indicated base:
$(42)_6 + (23)_6$

$$\begin{array}{r} (42)_6 \\ +\ (23)_6 \\ \hline (105)_6 \end{array}$$

10 PT.

5) Perform the following arithmetic operation in the indicated base:

$(5.3)_6 - (3.4)_6$

$$\begin{array}{r} {\scriptstyle 4\ +6} \\ (5.3)_6 \\ (3.4)_6 \\ \hline (1.5)_6 \end{array}$$

15 PT.

6) Perform the following operation in the indicated base:

$(5.3)_8 \times (3.5)_8$

$$\begin{array}{r} {\scriptstyle 1} \\ (5.3)_8 \\ (3.5)_8 \\ \hline \\ 3\ 2\ 7 \\ 2\ 0\ 1 \\ \hline (2\ 3\ .\ 3\ 7)_8 \end{array}$$

$15 \div 8 = 1 \quad R = 7$

$26 \div 8 = 3 \quad R = 2$

$9 \div 8 = 1 \quad R = 1$

$16 \div 8 = 2 \quad R = 0$

EGC220 **Quiz #1** *Dr. Izadi*

First NAME: Key **Last Name:**_____

1) Mark all that is correct

a. 0, 1 are valid entries in base 2
b. 1, 6, F are valid entries in base 16
c. 0, 1, 4 are valid entries in base 4
d. (205.6) is valid in base 7
e. (205.6) is valid in base 4
f. (2B5.E) is valid in base 12

2) Binary is base

a. 2
b. 4
c. 16
d. 8
e. 6

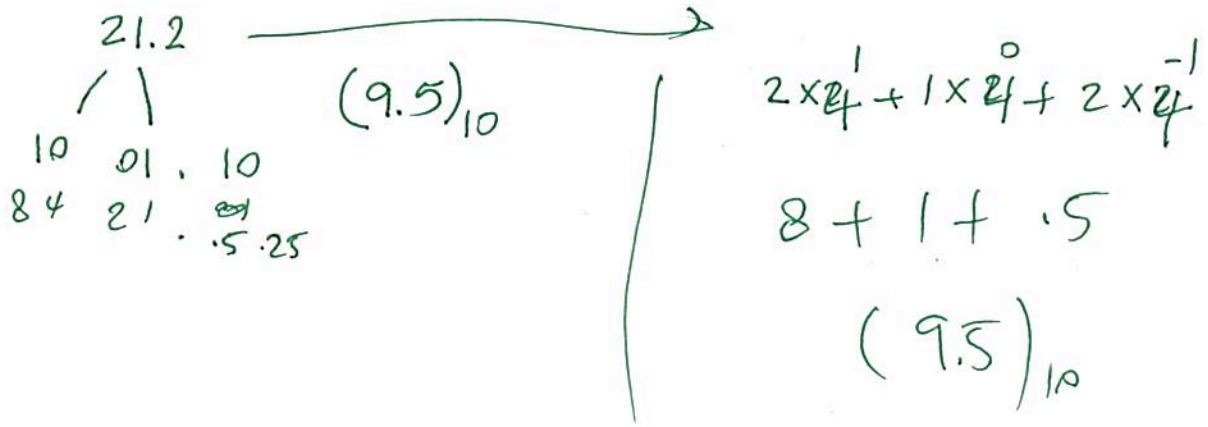
3) Hexadecimal is base

a. 2
b. 4
c. 16
d. 8
e. 6

4) Octal is base

a. 2
b. 4
c. 16
d. 8
e. 6

5) Convert $(21.2)_4$ to base 10



6) Convert $(E.6)_{16}$ to base 10

8 4 2 1 .5 .25 .125
1 1 1 0 . 0 1 1 0

$(14.375)_{10}$

$14 \times 16^{0} + 6 \times 16^{-1}$

$14 + .375$

$(14.375)_{10}$

7) Convert $(32.5)_{10}$ to base 4

32 16 8 4 2 1 . .5
1 0 0 0 0 0 . 1 0

2 0 0 . 2

$(200.2)_4$

---

b.

$32 \div 4 = 8 \quad R_0 = 0$

$8 \div 4 = 2 \quad R_1 = 0$

$2 \div 4 = 0 \quad R_2 = 2$

~~$\uparrow \div 2 = 0 \quad R_3 = 1$~~

$.5 \times 4 = 2.0$ ↑

$(200.2)_4$