Problem 1
Using D flip-flops, design a Moore based sequence detector with one input and one output, which would generate an output of 1 only when the input sequence is 101. Assume no overlapping.

Problem 2
Write a Verilog code for Problem 1

Problem 3
Using JK flip-flops, design a Mealy based sequence detector with one input and one output, which would generate an output of 1 only when the input sequence is 101. Assume no overlapping.

Problem 4
Write a Verilog code for Problem 3. Use default flip-flop given by Verilog.

Problem 5
Using D flip-flops, design a Moore based sequence detector with one input and one output, which would generate an output of 1 only when the input sequence is 101. Assume overlapping.

Problem 6
Write a Verilog code for Problem 5. Use default flip-flop given by Verilog.

Problem 7
Using JK flip-flops, design a Mealy based sequence detector with one input and one output, which would generate an output of 1 only when the input sequence is 101. Assume overlapping.

Problem 8
Write a Verilog code for Problem 7. Use default flip-flop given by Verilog.