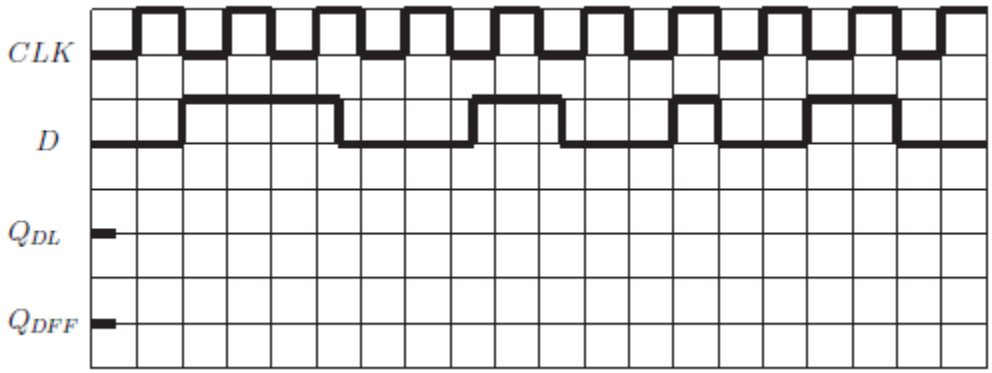
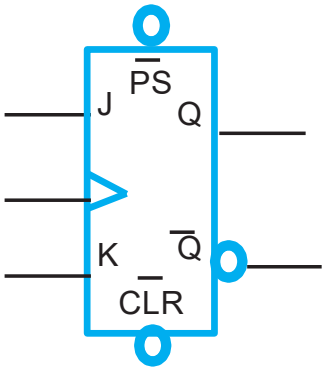
Problem 1

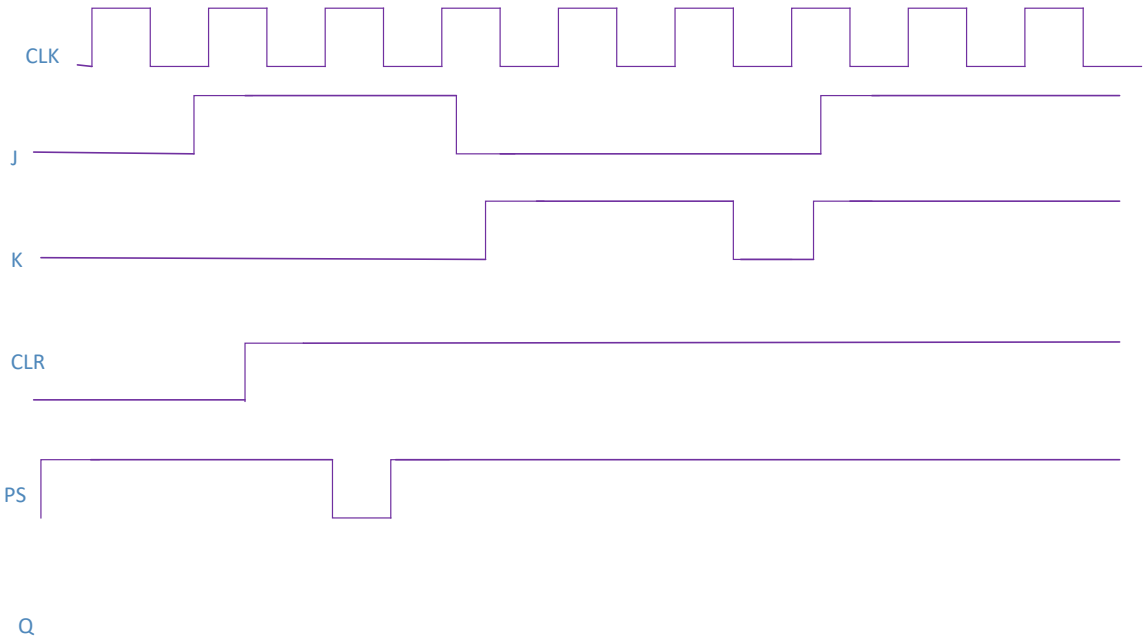
On the following graph, inputs CLK and *D* are shown. They are inputs to both a D latch and a D flip-flop. CLK goes into the active high G input ofthe D latch and positive edge clock input of the D flip-flop. Show the output of the D latch as Q_{DL} on the graph and the output of the D flip-flop as Q_{DFF} on the graph. Both outputs are initially o at the start of the graph, as shown. Do the two outputs differ, and if so, why?



Problem 2

Complete the following timing diagram for a JK flip-flop with a low active preset (PS) and clear (CLR).





Problem 3
Using T flip-flops, design a ripple counter that counts 0 – 7 and repeats.

Problem 4
Show the waveform diagram for the counter in Problem 3.