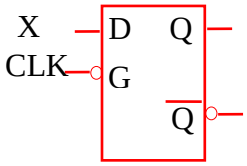
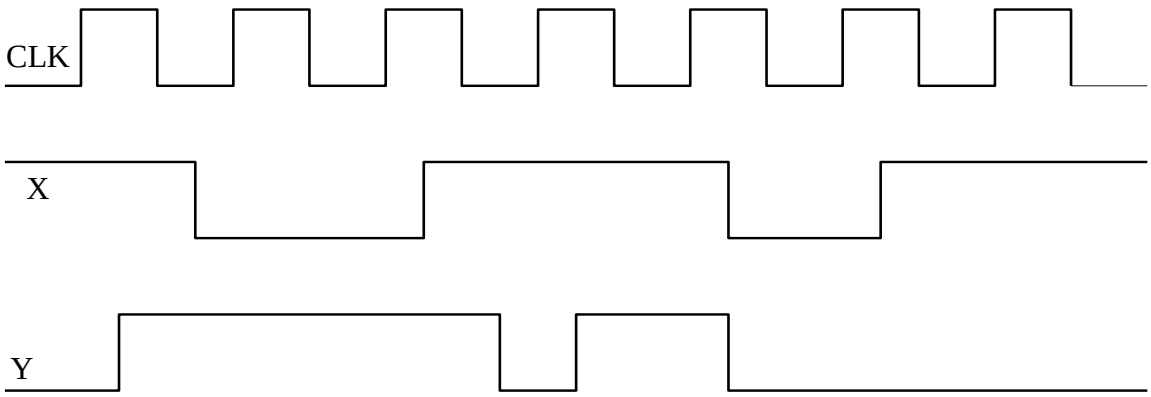
Problem 1
Using Verilog, design an ALU with the following specification:

S	Function
0	A-B
1	A+B
2	A + 1
3	A - 1
4	A AND B
5	A OR B
6	A XOR B
7	A’

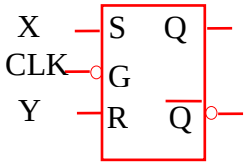
Problem 2
Complete the timing diagram if the following signals are applied as indicated.

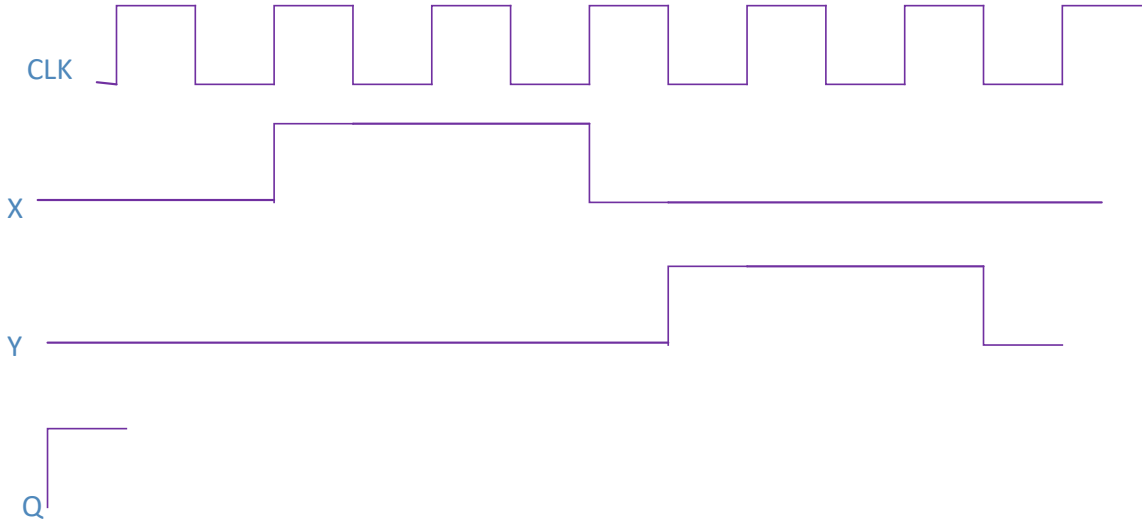




Problem 3

Complete the timing diagram if the following signals are applied as indicated.





Problem 4

Complete the timing diagram if the following signals are applied as indicated.