Problem 1
There is an integrated circuit called a BCD-seven segment decode that takes 4 inputs and has seven output. The inputs represent a number between 0 and 9 , and each of the seven outputs corresponds to one of seven LED's in a seven-segment display. A typical seven segment display is shown below.


The other digits are formed as described in this table.

| Digit | Inputs |  |  |  | $\begin{gathered} \text { Output } \\ (7 \\ \text { Segments) } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | D | C | B | A |  |
| 0 | 0 | 0 | 0 | 0 | $\overline{11}$ |
| 1 | 0 | 0 | 0 | 1 | ! |
| 2 | 0 | 0 | 1 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | I |
| 4 | 0 | 1 | 0 | 0 | 11 |
| 5 | 0 | 1 | 0 | 1 | I |
| 6 | 0 | 1 | 1 | 0 | 5 |
| 7 | 0 | 1 | 1 | 1 | $7$ |
| 8 | 1 | 0 | 0 | 0 | $\overline{\mathrm{II}}$ |
| 9 | 1 | 0 | 0 | 1 | $\frac{I}{1}$ |

a. Write the truth table for each segment "a, b, c, d, e, f, g" with inputs A, B, C, and D. Make sure to adhere to the indicated segment notations.
b. Simplify each output in Minimum S.O.P.
c. Implement each output using all NAND gates.

## Problem 2

Design a 1 out of 4 decoder with active low outputs and two enable lines, one active low and one active high.

Problem 3
Using the decoder in Problem 2, design a 1 out of 16 decoder with active low outputs.
Problem 4
Write a Verilog code for the decoder in Problem 2.

