EGC220 Practice Problems for Exam 2

1. Circle T (true) or F (false) for each of these Boolean equations.

(a). T F An 8-to-1 multiplexer requires 2 select lines.
(b). T F A half adder has a carry input.
(c). T F Even parity means the data has an even number of bits that are 1 .
(d). T F If a decoder has 16 outputs, it requires 3 inputs to choose all possible outputs.

2. Combinational Circuit Design

(a) Design a circuit that would detect whether the 4 input has odd parity.

(b) Design a circuit that counts the number of 1's present in 3 inputs A, B and C. Its output is a two-bit number X1X0, representing that count in binary. Assume active-HIGH logic.

3. Combinational Logic: Multiplexers and Encoders

(a).Draw a block diagram of a 4-to-1 multiplexer and indicate its truth table. Show the internal circuitry using all NAND gates.

(b) Draw a block diagram of a 2-to-4 decoder with two active low enables lines and active high outputs and indicate its truth table. Show the internal circuitry.

(b).Draw a block diagram of a 4-to-2 priority encoder. Label all inputs and outputs. How is the 4-to-2 encoder different from a 4-to-1 multiplexer?

4. Combinational Logic: Binary Adders

You wish to add two 4-bit numbers. You have half adders and full adders available to use as components. Draw a block diagram of your 4-bit adder, using half and full adders. Do not draw a gate-level diagram. Show and label all inputs and outputs.

5. Prove or disprove that 1-0ut of 8 decoder is the same as 1 × 8 DeMUX.

6. Sequential Logic: Latches and Flip-flops

(a) Draw a gate-level diagram of a D latch with low active gate input. Show and label all inputs and outputs.

(b). Draw a block diagram of the following devices and label all synchronous and asynchronous inputs. Moreover, write an appropriate characteristic table for each device.

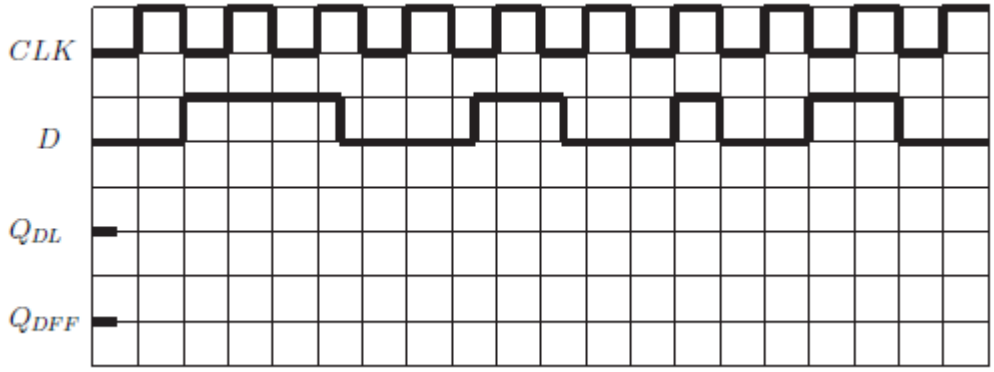
i. D flip-flop

ii. T flip-flop

iii. JK flip-flop

iv. SR flip-flop

(c). On the following graph, inputs CLK and *D* are shown. They are inputs to both a D latch and a D flip-flop. CLK goes into the Gate or Clock input. Write the output of the D latch as Q_{DL} on the graph. Then write the output of the D flip-flop as Q_{DFF} on the graph. Both outputs are initially 0 at the start of the graph, as shown. Do the two outputs differ, and if so, why?

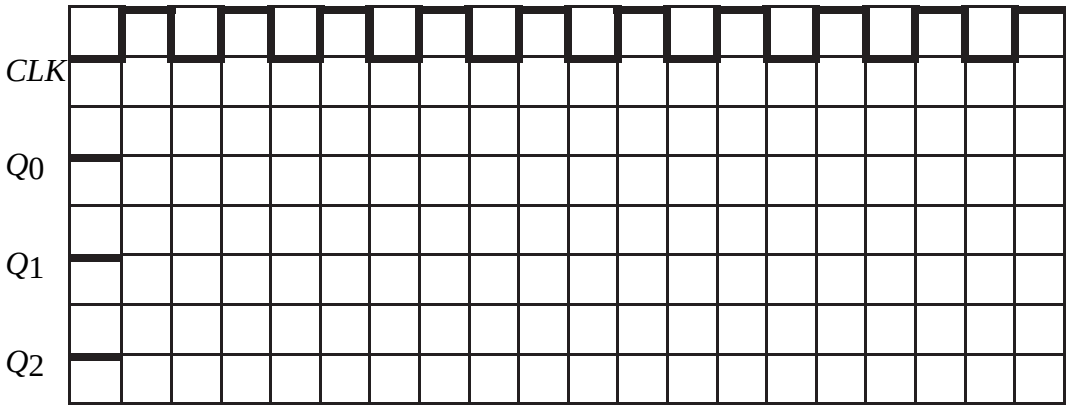


7. Counters

(a). Design a ripple counter using J-K flip-flops, which counts 11 - 6.

(b). Design a ripple counter using D flip-flops, which counts 6 - 3.

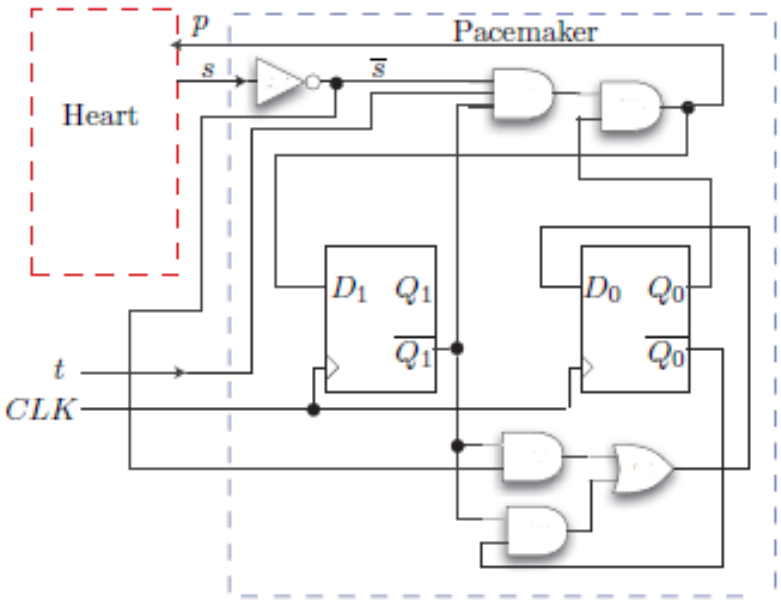
(c). For the ripple counter in part b, show the output Q_0, Q_1 and Q_2 in the grid below. Assume Q_0 to be the least significant bit and the initial count be 6.



8. Analysis of FSM Circuit Design

Below is a simplified block diagram of a heart pacemaker. The output p from the pacemaker pulses high if the heart does not contract within a certain time. The input s indicates whether the heart has contracted (s = 1) or not (s = 0). The input t comes from a timer, which counts for the expected time between contractions (approximately 1 second). When t = 1, the timer has counted up to 1 second, and the heart should have contracted. If the heart has not contracted within that time, the pacemaker sends a pulse p = 1. (There is also a timer reset control coming from the pacemaker, which we ignore for this problem.)

The inputs to the pacemaker circuit are s (from the heart) and t (from a timer - not shown). The output of the pacemaker circuit is p, which goes to the heart. Arrows indicate the inputs and output.



a. Analyze the circuit leading to a state diagram.

b. Is this a Mealy or a Moore machine? Why?