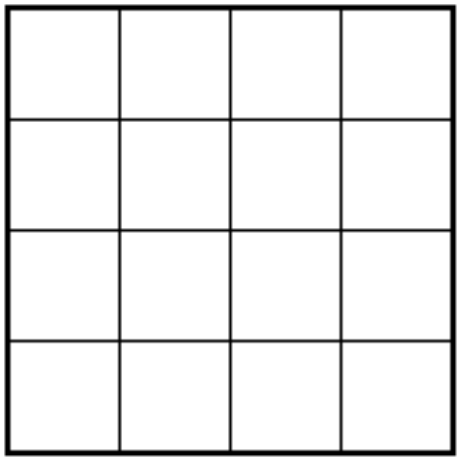
EGC220 Practice Problems for Exam 2

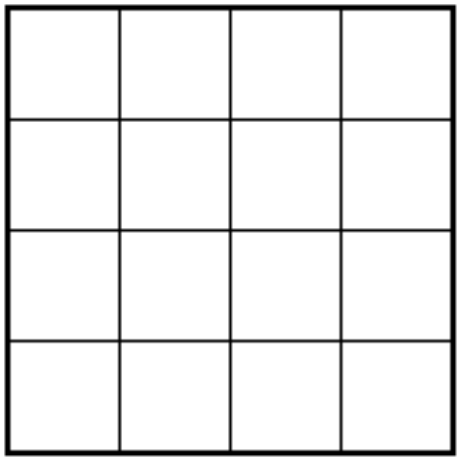
1. Circle T (true) or F (false) for each of these Boolean equations.

(a). T F An 8-to-1 multiplexer requires 2 select lines.
(b). T F A half adder has a carry input.
(c). T F Even parity means the data has an even number of bits that are 1 .
(d). T F If a decoder has 16 outputs, it requires 3 inputs to choose all possible outputs.

2. For $Y = f(w, x, y, z) = \Pi M(0, 1, 2, 3, 5, 8, 9, 13)$
(a). Fully label and complete the Karnaugh map below with Y as given above. Then derive a minimized POS expression for $Y = f(w, x, y, z)$.



(b). Fully label and complete the Karnaugh map below with Y as given above. Then derive a minimized SOP expression for Y.



3. Combinational Logic:

Design a circuit that counts the number of 1's present in 3 inputs A, B and C. Its output is a two-bit number X_1X_0, representing that count in binary. Assume active-HIGH logic.

(a) Write the truth table for this circuit.

3(b). Find the minimized logic equations for outputs X_1 and X_0; use a K-map if needed.

3(c). Draw the corresponding logic diagram for this circuit. Label all inputs and outputs.

4. Combinational Logic: Multiplexers and Encoders

4(a).Draw a block diagram of a 4-to-1 multiplexer. Do not use a gate-level diagram. Label all inputs and outputs.

4(b).Draw a block diagram of a 4-to-2 encoder. Label all inputs and outputs. How is the 4-to-2 encoder different from a 4-to-1 multiplexer?

4(c).Write the truth table for a 4-to-2 priority encoder.

4(d) Write a simplified truth table for a 4-to-1 multiplexer (hint: your multiplexer truth table should have 2 inputs).

5. Combinational Logic: Binary Adders

You wish to add two 4-bit numbers. You have half adders and full adders available to use as components.Draw a block diagram of your 4-bit adder, using half and full adders. Do not draw a gate-level diagram. Show and label all inputs and outputs.

6. Prove or disprove that 1-0ut of 8 decoder is the same as 1 × 8 DeMUX.