# SUNY NEW PALTZ

**Department of Electrical and Computer Engineering**

**CSE 45493 - 3 Functional Verification of Hardware Designs (3 credits)**
**Fall 2003 Semester**

## COURSE SYLLABUS

## 1. GENERAL INFORMATION


Professors: Dr. Baback Izadi
IBM: Bruce Wile, Dean Bair, Kurt Schweiger, Jim Schafer, Rebecca Gott, Steve Mittermaier, John Aylward

Office: 203 Resnick Engineering Hall
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Office hours: Monday 1:00 - 3:00 PM
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and by appointment

Class time and place: Monday and Wednesday
10 AM - 11:15 AM

Teaching Assistant:
REH 211

Relevant Web Pages:
Course: http://www.engr.newpaltz.edu/~bai/CSE45493/cse45493.html
Verification Related http://janick.bergeron.com/wtb

Textbook: *Writing Testbenches: Functional Verification of HDL Models*, J. Bergeron, Kluwer Academic Publishers, 2000, ISBN 0-79233-7766-4

References: *A Designers Guide to VHDL*, Peter Ashenden,

Prerequisite: Digital Logic Fundamentals (CSE-45230 and CSE-45208) and basic knowledge of VHDL.

## 2. COURSE OBJECTIVES

Techniques for verification of hardware designs; writing testbenches; verification of increasingly complex computer circuit designs provided by industry using simulation environments used in industry.

The Course objectives are:

(i) Students will learn to plan and carry out an effective functional verification of a design.
(ii) Students will learn to use verification tools and experiment on actual circuits designed in industry.
(iii) Student will learn to work in teams to debug designs.

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| ***NOTE:*** | ***At the end of the semester, students will evaluate how these course objectives have been met.*** |

## 3. COURSE CONTENTS

| Lecture Number | Date | Lecture Title | Instructor(s) | Reading Assignments |
|---|---|---|---|---|
| 1 | 8/25 | Introduction, Course Overview, Industry Perspective | Izadi<br>Wile | Chapter 1 |
| 2 | 8/27 | Verification Process/Cycle | Izadi | Chapter 3 |
| 3 | 9/4 | Model Tech usage (User interface, waveform viewer)<br>(Class held in UNIX Lab) | Yang | Chapter 2 |
| 4 | 9/9 | Lab 1 introduction, Testplans/Testcases/Testbenches | Wile/Izadi | Chapter 3 |
| 5 | 9/11 | Driving Stimulus and simple checking (Line Delete example) | Bair | Chapter 5 |
| 6 | 9/18 | Simulation Engines | Schweiger | Chapter 2 |
| 7 | 9/23 | Lab1 Review/Solution Discussion<br>…assignment: Escape Analysis | Izadi/Wile | |
| 8 | 9/25 | Random methodologies vs. Deterministic | Izadi | Chapter 5 |
| 9 | 9/30 | Introduction to “e” /Verisity Tutorial | Izadi | |
| 10 | 10/2 | Continued “e” discussions and introduce Lab 2 | Izadi | |
| 11 | 10/7 | Strategies for driving testcases | Schafer | Chapter 5,6 |
| 12 | 10/9 | Strategies for checking | Bair | Chapter 5,6 |
| 13 | 10/16 | Mid-term Exam | | |
| 14 | 10/21 | Formal Verification introduction | Gott | |
| 15 | 10/23 | Lab 2 Review/Solutions/Escape Analysis | Wile | |
| 16 | 10/28 | Formal Verification<br>Genbuf example (in class) | Izadi | |

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| 17 | 10/30 | Formal Verification (lab…re-run Lab 1 using Rulebase) | Izadi | |
| 18 | 11/4 | Formal Verification | Izadi | |
| 19 | 11/6 | Formal Verification (Quiz/Exam) | Izadi | |
| 20 | 11/11 | Lab 3 (Course Project) Introduction, team assignments | Izadi | |
| 21 | 11/13 | Advanced Specman features | Izadi | |
| 22 | 11/18 | Coverage | Mittermaier | Chapter 2 |
| 23 | 11/20 | Coverage Driven Feedback | Aylward | |
| 24 | 11/25 | Testcase Generation | Izadi | |
| 25 | 12/2 | Pervasive Function Verification | Izadi | |
| 26 | 12/4 | Case study (BHT) | Izadi | |
| 27 | 12/9 | How do you know when you're done? | Izadi | Chapter 7 |
| 28 | 12/10 | (Tuesday!) Lab 3 Completion/Review/Solutions/Discussion | Izadi | |
| | | Final Exam | | |

## 4. GRADING POLICY

### 4.1. Grade Distribution

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|---|---|
| Labs and Projects: | 300 Points |
| Mid-term exams: | 100 Points |
| Final Exam: | 100 Points |

### 4.2. Course Rules and General Comments:

- Any disputed grade must be resolved within 7 days of the return of the graded item. Please check with the teaching assistant first and then with the instructor if needed.
- You are responsible for all the course materials and all lecture contents unless specified otherwise by the instructor. If you miss a class, it is your responsibility to obtain assignments and other information given on that day.
- All your coursework (lab assignments, project, and exams) is expected to be your own. Evidence indicating copying of work or other cooperation will be dealt with based on university academic conduct rules. General instructions such as assisting in problem interpretation, and giving of occasional hints on problem attack (i.e., the kind of help you would get from the instructor or a teaching assistant in the course!), however, are permitted.
- Save your graded homework, tests, and project report. I may ask for them in case of any grade discrepancy.

## 5. RELATIONSHIP BETWEEN COURSE OBJECTIVES AND PROGRAM'S OBJECTIVES

This section is of an informative character. First, it states the common educational objectives of the Electrical and Computer Engineering Programs. Second, for the sake of clarity, it restates the course objectives of section 2, and third, it establishes the connection between program and course objectives.

### 5.1. Program's Educational Objectives:

**I) Fundamental Knowledge:** The Electrical and Computer Engineering Programs will provide students with fundamental knowledge of mathematics, Sciences and engineering, in order for them to apply this knowledge to the solution of electrical engineering problems.

**II) Design and Practical Skills:** The Electrical and Computer Engineering Programs will enable students to perform engineering design subject to engineering standards and constrains. In addition, the program will provide students with hands-on experience for implementing such designs.

**III) Social and Professional Aptitude:** The Electrical and Computer Engineering Programs will provide a broad-based education which instill in our diverse student body professional and ethical conduct, communication and teamwork skills, and the desire for life-long learning to interact effectively with the members of engineering profession as well as society at large.

### 5.2. Course Objectives

(i) Students will learn to plan and carry out an effective functional verification of a design.
(ii) Students will learn to use verification tools and experiment on actual circuits designed in industry.
(iii) Student will learn to work in teams to debug designs.

### 5.3 Link between Course Objectives and Program Objectives

| Course Objective | Contributes to | Program Objective |
|---|---|---|
| (i) | → | 1 |
| (ii) | → | 1 & 2 |
| (iii) | → | 2 & 3 |