ModelSim®

PE

Tutorial

Version 5.6

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The world's most popular HDL simulator

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Introduction

Chapter contents

Software versions

This documentation was written to support ModelSim PE 5.6 for Microsoft Windows 98/Me/NT/2000/XP. If the ModelSim software you are using is a later release, check the README file on the CD-ROM that accompanied the software. Any supplemental information will be there.

Although this document covers both VHDL and Verilog simulation, you will find it a useful reference even if your design work is limited to a single HDL.

Standards supported

ModelSim VHDL supports both the IEEE 1076-1987 and 1076-1993 VHDL, the 1164-1993 *Standard Multivalue Logic System for VHDL Interoperability*, and the 1076.2-1996 *Standard VHDL Mathematical Packages* standards. Any design developed with ModelSim will be compatible with any other VHDL system that is compliant with either IEEE Standard 1076-1987 or 1076-1993.

ModelSim Verilog is based on IEEE Std 1364-1995 and a partial implementation of 1364-2001 (see */<install_dir>/modeltech/docs/technotes/vlog_2000.note* for implementation details) *Standard Hardware Description Language.* The Open Verilog International *Verilog LRM version 2.0* is also applicable to a large extent. Both PLI (Programming Language Interface) and VCD (Value Change Dump) are supported for ModelSim PE and SE users.

In addition, all products support SDF 1.0 through 3.0, VITAL 2.2b, VITAL'95 – IEEE 1076.4-1995, and VITAL 2000 – IEEE 1076.4-2000.

Assumptions

We assume that you are familiar with the use of your operating system. If you are not familiar with Microsoft Windows, we recommend that you work through the tutorials provided with MS Windows before using Model*Sim*.

We also assume that you have a working knowledge of VHDL and Verilog. Although ModelSim is an excellent tool to use while learning HDL concepts and practices, this document is not written to support that goal.

Where to find our documentation

ModelSim documentation is available from our website at www.model.com/support/documentation.asp or in the following formats and locations:

Document	Format	How to get it
Start Here for ModelSim PE (installation & support reference)	paper	shipped with ModelSim
	PDF	select **Main window > Help >PE Documentation**; also available from the Support page of our web site: www.model.com
ModelSim PE Quick Guide (command and feature quick-reference)	paper	shipped with ModelSim
	PDF	select **Main window > Help >PE Documentation**, also available from the Support page of our web site: www.model.com
ModelSim PE Tutorial	PDF, HTML	select **Main window > Help >PE Documentation**; also available from the Support page of our web site: www.model.com
ModelSim PE User's Manual	PDF, HTML	select **Main window > Help >PE Documentation**
ModelSim PE *Command Reference*	PDF, HTML	select **Main window > Help >PE Documentation**
Std_DevelopersKit User's Manual	PDF	www.model.com/support/pdf/sdk_um.pdf The Standard Developer's Kit is for use with Mentor Graphics QuickHDL.
ModelSim Command Help	ASCII	type `help [command name]` at the prompt in the Main window
Error message help	ASCII	type `verror <msgNum>` at the prompt in the Main window or at a shell prompt
Tcl Man Pages (Tcl manual)	HTML	select **Main window > Help > Tcl Man Pages**, or find *contents.htm* in *\modeltech\docs\tcl_help_html*
application notes	HTML	www.model.com/resources/techdocs.asp
frequently asked questions	HTML	www.model.com/resources/faqs.asp

Document	Format	How to get it
tech notes	ASCII	select **Main window > Help > Technotes**, or located in the *\modeltech\docs\technotes* directory

Technical support and updates

The Model Technology web site includes links to support, software updates, and many other information sources.

Support

www.model.com/support/default.asp

Customers in Europe should contact their distributor for support. See www.model.com/contact_us.asp for distributor contact information.

Updates

www.model.com/products/release.asp

Latest version email

Place your name on our list for email notification of news and updates.
www.model.com/support/register_news_list.asp

Before you begin

Preparation for some of the lessons leaves certain details up to you. You will decide the best way to create directories, copy files and execute programs within your operating system. (When you are operating the simulator within ModelSim's GUI, the interface is consistent for all platforms.)

Additional details for VHDL, Verilog, and mixed VHDL/Verilog simulation can be found in the *ModelSim User's Manual* and *Command Reference*. (See "Where to find our documentation" (T-7).)

Command, button, and menu equivalents

Many of the lesson steps are accomplished by a button or menu selection. When appropriate, VSIM command line (PROMPT:) or menu (MENU:) equivalents for these selections are shown in parentheses within the step. This example shows three options to the **run -all** command, a button, prompt command, and a menu selection.

(PROMPT: run -all) (MENU: Simulate > Run > Run -All)

Drag and drop

Drag and drop allows you to copy and move signals among windows. If drag and drop applies to a lesson step, it is noted in a fashion similar to MENUS and PROMPTS with: DRAG&DROP.

Command history

As you work on the lessons, keep an eye on the Main transcript window. The commands invoked by buttons and menu selections are echoed there. You can scroll through the command history with the up and down arrow keys, or the command history may be reviewed with several shortcuts at the ModelSim/VSIM prompt.

Shortcut	Description
click on prompt	left-click once on a previous ModelSim or VSIM prompt in the transcript to copy the command typed at that prompt to the active cursor
`his or history`	shows the last few commands (up to 50 are kept)

Reusing commands from the Main transcript

ModelSim's Main transcript can be saved, and the resulting file used as a DO (macro) file to replay the transcribed commands. You can save the transcript at any time before or during simulation. You have the option of clearing the transcript (File > Transcript > Clear Transcript) if you don't want to save the entire command history.

To save the contents of the transcript select **File > Transcript > Save Transcript As** from the Main menu.

Replay the saved transcript with the **do** command:

```
do <do file name>
```

For example, if you saved a series of compiler commands as *mycompile.do* (the .do extension is optional), you could recompile with one command:

```
do mycompile.do
```

Note: Neither the prompt nor the Return that ends a command line are shown in the examples.

Lesson 1 - Creating a Project

The goals for this lesson are:

- Create a project

A project is a collection entity for an HDL design under specification or test. Projects ease interaction with the tool and are useful for organizing files and simulation settings. At a minimum, projects have a work library and a session state that is stored in a .mpf file. A project may also consist of:

- HDL source files or references to source files
- other files such as READMEs or other project documentation
- local libraries
- references to global libraries

For more information about using project files, see the *ModelSim User's Manual*.

1 Start ModelSim with one of the following:

for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

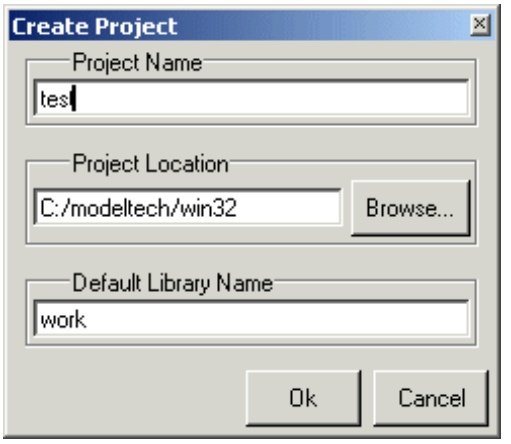
```
modelsim.exe
```

Note: if you didn't add ModelSim to your search path during installation, you will have to include the full path when you type this command at a DOS prompt.

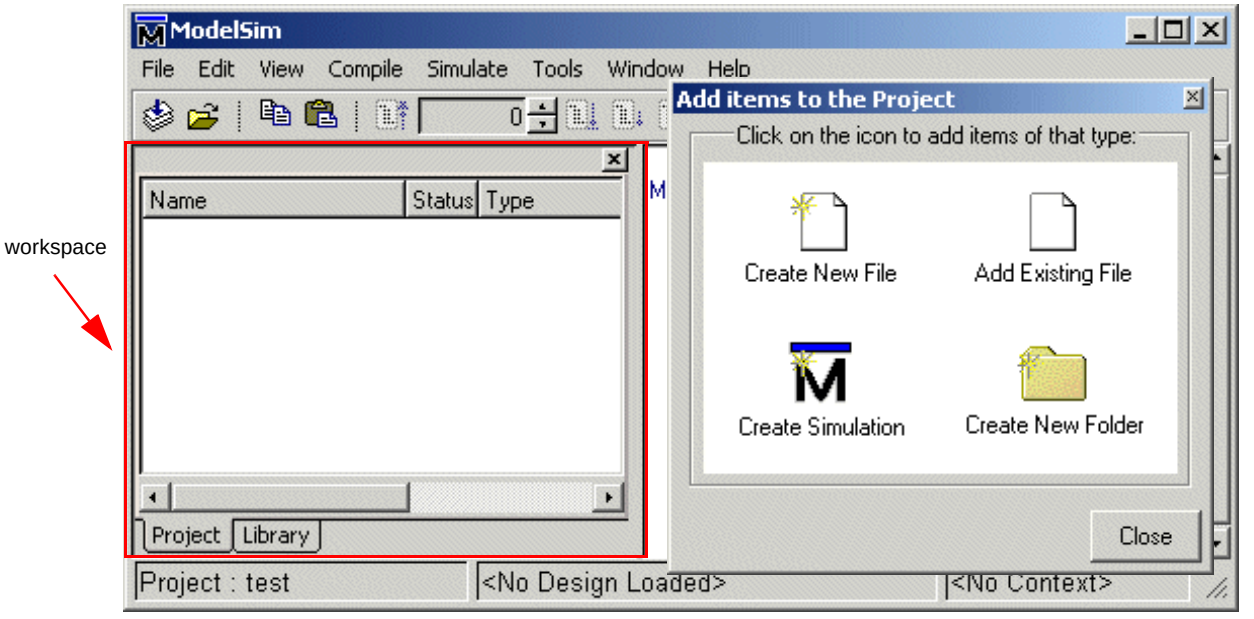
Upon opening ModelSim for the first time, you will see the **Welcome to ModelSim** dialog. (If this screen is not available, you can enable it by selecting **Help > Welcome Menu** from the Main window. It will then display the next time you start ModelSim.)

You can access a variety of information about ModelSim via this dialog. For now click **Close** to dismiss the dialog.

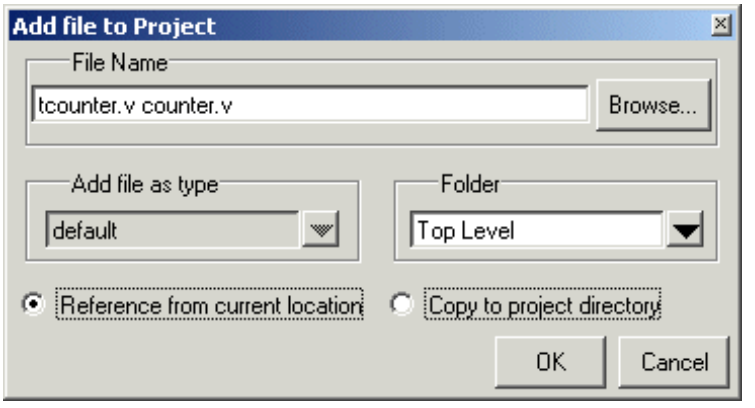
2 Select **File > New > Project** (Main window). In the **Create Project** dialog box, enter "test" as the Project Name and select a directory where the project file will be stored. Leave the Default Library Name set to "work."



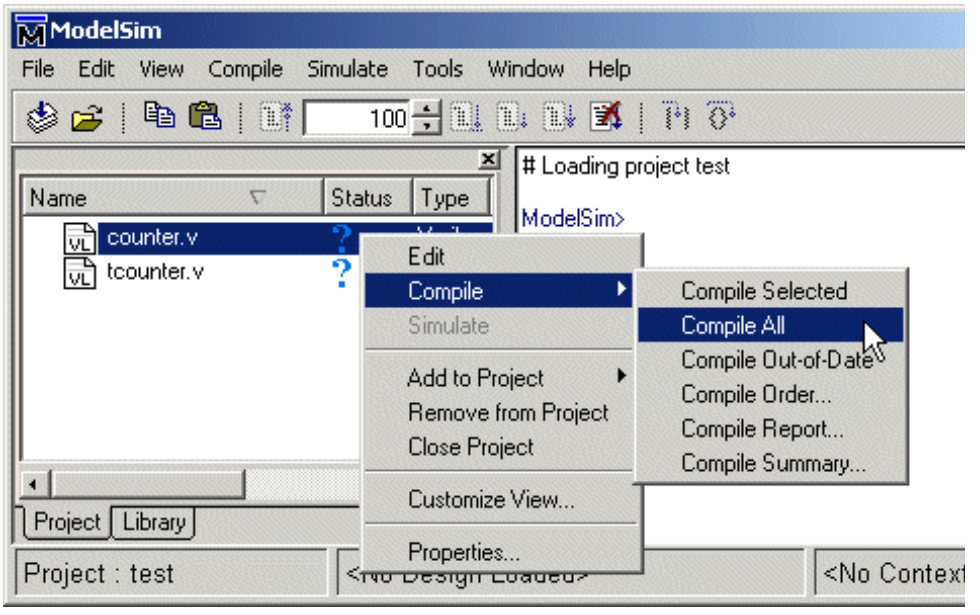
Upon selecting OK, you will see a blank Project tab in the workspace area of the Main window and the **Add Items to the Project** dialog.



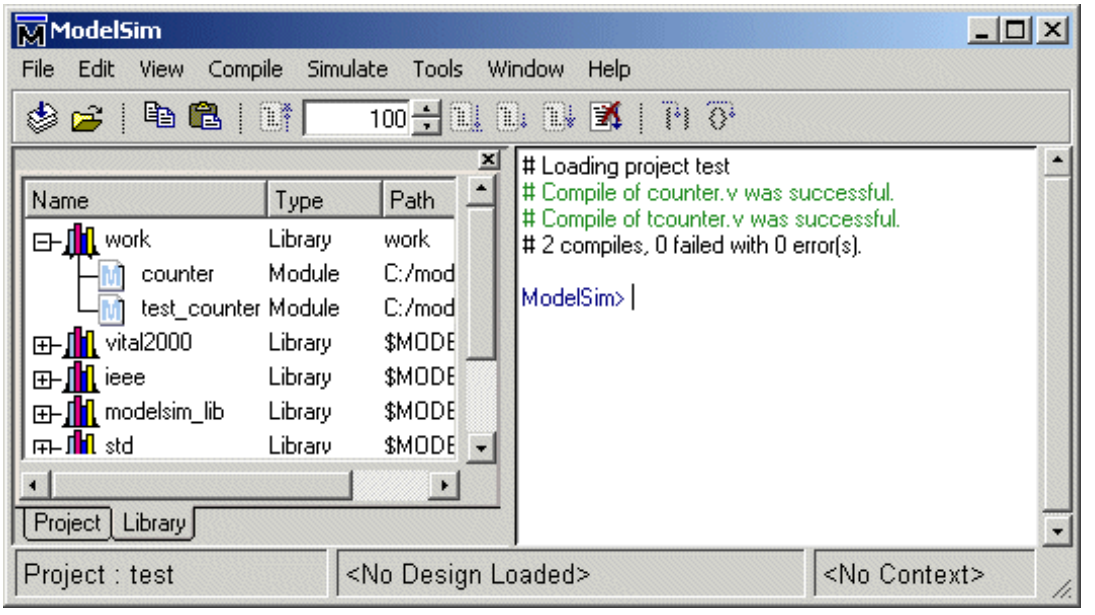
3 The next step is to add the files that contain your design units. Click **Add Existing File** in the **Add Items to Project** dialog. For this exercise, we'll add two Verilog files. Click the **Browse** button in the Add file to Project dialog box and open the examples directory in your ModelSim installation. Select *tcounter.v* and *counter.v*. Select **Reference from current location** and then click OK.



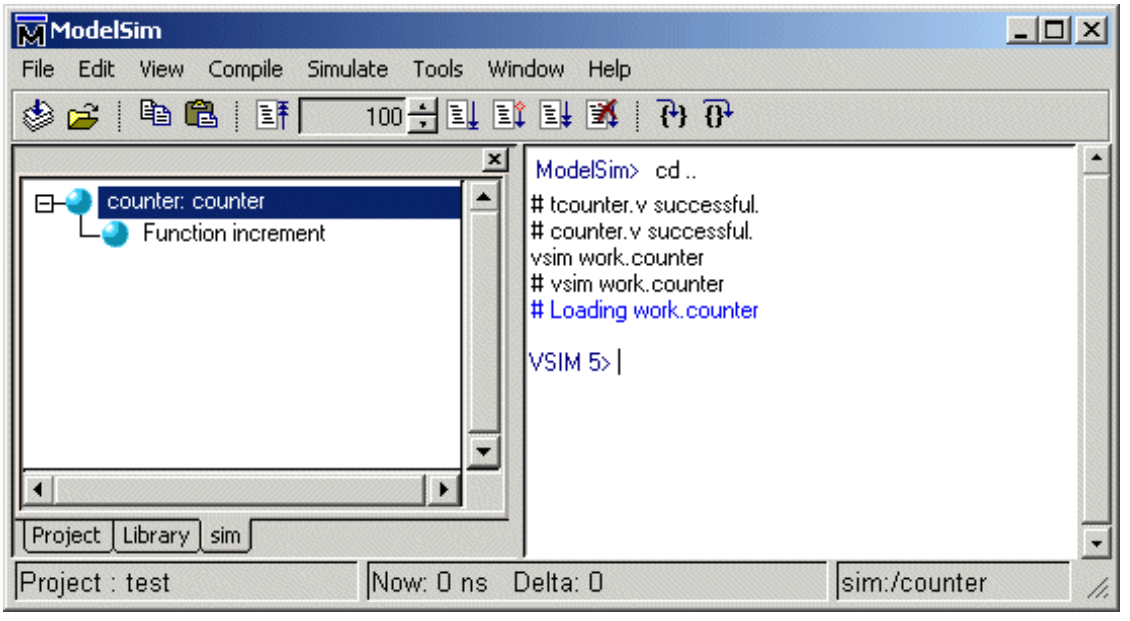
4 Click your right mouse button (2nd button in Windows; 3rd button in UNIX) in the Project page and select **Compile > Compile All**.



5 The two files are compiled. Click on the Library tab and expand the *work* library by clicking the "+" icon. You'll see the compiled design units listed.



6 The last step in this exercise is to load one of the design units. Double-click *counter* on the Library page. You'll see a new page appear in the Workspace that displays the structure of the *counter* design unit.



At this point, you would generally run the simulation and analyze or debug your design. We'll do just that in the upcoming lessons. For now, let's wrap up by ending the simulation and closing the project. Select **Simulate > End Simulation** and confirm

that you want to quit simulating. Next, select **File > Close > Project**, confirm that you want to close the project, and select **Yes** to update your project file with the changes you made during this session.

Note that a *test.mpf* file has been created in your working directory. This file contains information about the project *test* that you just created. ModelSim will open this project automatically the next time you invoke the tool.

Lesson 2 - Basic VHDL simulation

The goals for this lesson are:

- Create a library and compile a VHDL file
- Load a design
- Learn about the basic ModelSim windows, mouse, and menu conventions
- Force the value of a signal
- Run ModelSim using the **run** command
- Set a breakpoint
- Single-step through a simulation run

The project feature covered in Lesson 1 executes several actions automatically such as creating and mapping work libraries. In this lesson we will go through the entire process so you get a feel for how ModelSim really works.

Compiling the design

1 Start by creating a new directory for this exercise (in case other users will be working with these lessons). Create the directory, then copy all of the VHDL (.vhd) files from *\<install_dir\>\modeltech\examples* to the new directory.

Make sure the new directory is the current directory. Do this by invoking ModelSim from the new directory or by selecting **File > Change Directory** (Main window).

2 Start ModelSim with one of the following:

for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

```
modelsim.exe
```

Note: If you didn't add ModelSim to your search path during installation, you will have to include the full path when you type this command at a DOS prompt.

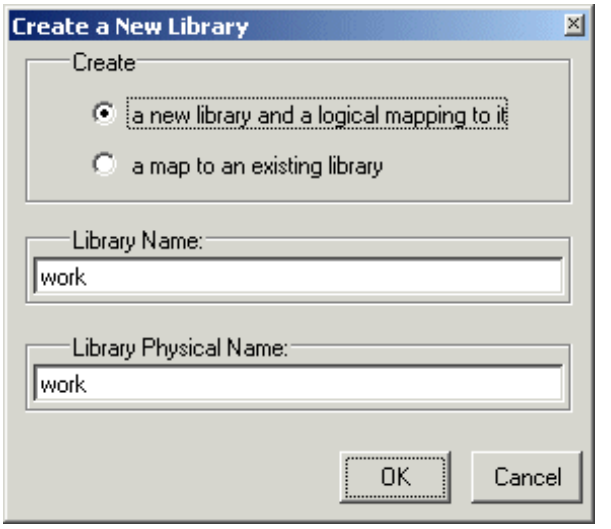
Select "Proceed to ModelSim" if the Welcome dialog appears.

3 Before you compile any HDL code, you'll need a design library to hold the compilation results. To create a new design library, make this menu selection in the Main window: **File > New > Library**.

Make sure **Create: a new library and a logical mapping to it** is selected. Type "work" in the Library Name field and then select **OK**.

This creates a subdirectory named *work* - your design library - within the current directory. ModelSim saves a special file named *_info* in the subdirectory.

(PROMPT: vlib work
vmap work work)

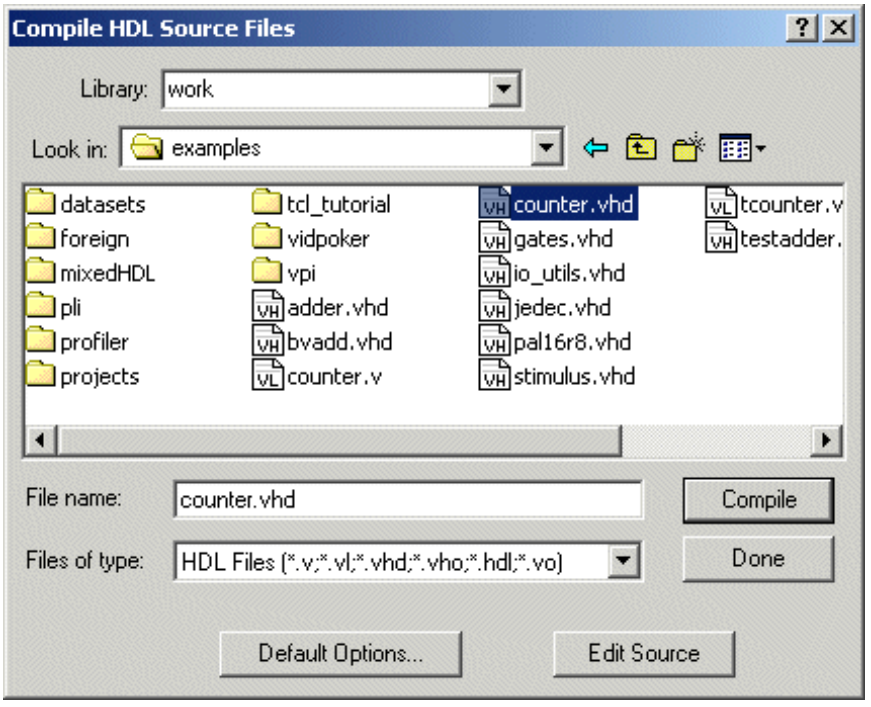


Note: Do not create a Library directory using Windows commands, because the *_info* file will not be created. Always use the File menu or the **vlib** command from either the ModelSim or DOS prompt.)

4 Compile the file *counter.vhd* into the new library by selecting **Compile** > **Compile**.

(PROMPT: vcom counter.vhd)

This opens the Compile HDL Source Files dialog box. (You won't see this dialog box if you invoke vcom from the command line.)



Complete the compilation by selecting *counter.vhd* from the file list and clicking **Compile**. Select **Done** when you are finished.

You can compile multiple files in one session from the file list. Individually select and compile the files in the order required by your design.

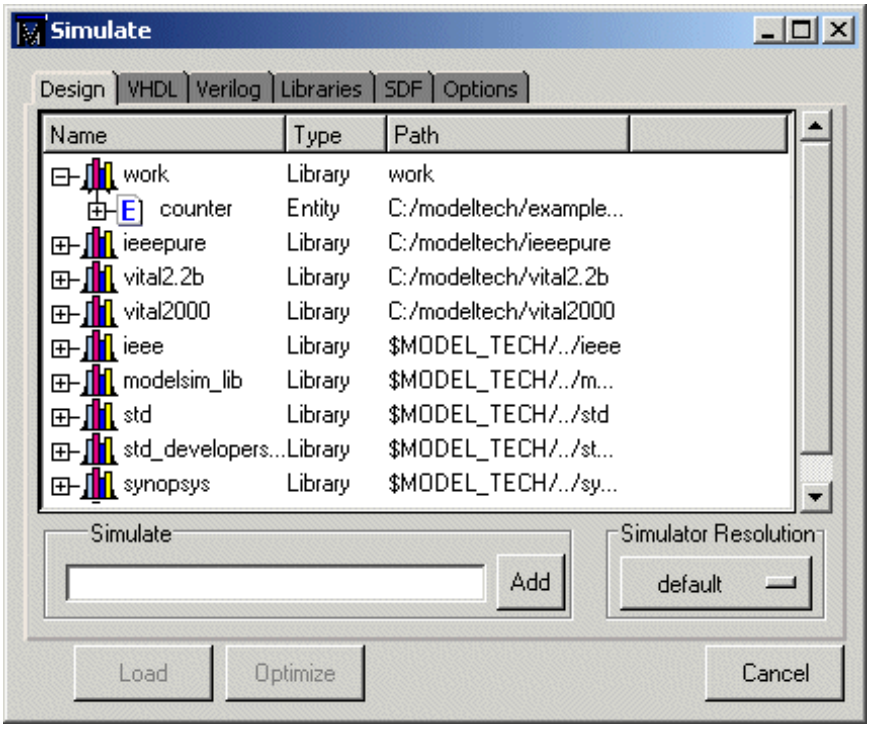
Note that you can have ModelSim determine the compile order. See "Auto-generating compile order" in the Project chapter of the *ModelSim User's Manual* for details.

Loading the design

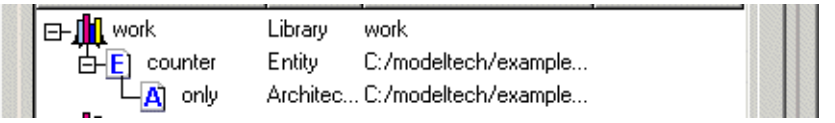
1 Load the design unit by selecting **Simulate > Simulate**.

(PROMPT: vsim counter)

The Simulate dialog box appears. Click the "+" sign next to 'work' to see the **counter** design unit. (You won't see this dialog box if you invoke **vsim** with *counter* from the command line.)



If the Design Unit is an entity (like **counter** in this design), you can expand it to view any associated architectures.



Select the entity **counter** and choose **Load**.

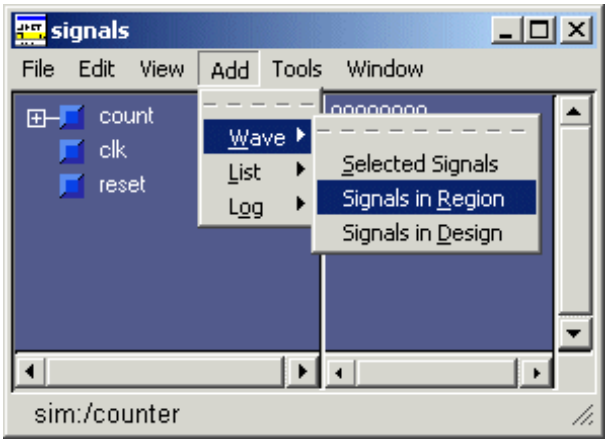
2 Next, select **View > All Windows** from the Main window menu to open all ModelSim windows.

(PROMPT: view *)

For descriptions of the windows, consult the *ModelSim User's Manual*.

3 Next let's add top-level signals to the Wave window by selecting **Add** > **Wave** > **Signals in Region** from the Signals window menu.

(PROMPT: add wave /counter/*)



Running the simulation

We will start the simulation by applying stimulus to the clock input.

1 Click in the Main window and enter the following command at the VSIM prompt:

```
force clk 1 50, 0 100 -repeat 100
```

(Signals MENU: Edit > Clock)

ModelSim interprets this **force** command as follows:

- force clk to the value 1 at 50 ns after the current time
- then to 0 at 100 ns after the current time
- repeat this cycle every 100 ns

2 Now you will exercise two different **Run** functions from the toolbar buttons on either the Main or Wave window. (The **Run** functions are identical in the Main and Wave windows.) Select the **Run** button first. When the run is complete, select **Run -All**.

Run. This causes the simulation to run and then stop after 100 ns.
(PROMPT: run 100) (Main MENU: Simulate > Run > Run 100ns)

Run -All. This causes the simulator to run forever. To stop the run, go on to the next step.
(PROMPT: run -all) (Main MENU: Simulate > Run > Run -All)

3 Select the **Break** button on either the Main or Wave toolbar to interrupt the run. The simulator will stop running as soon as it gets to an acceptable stopping point.

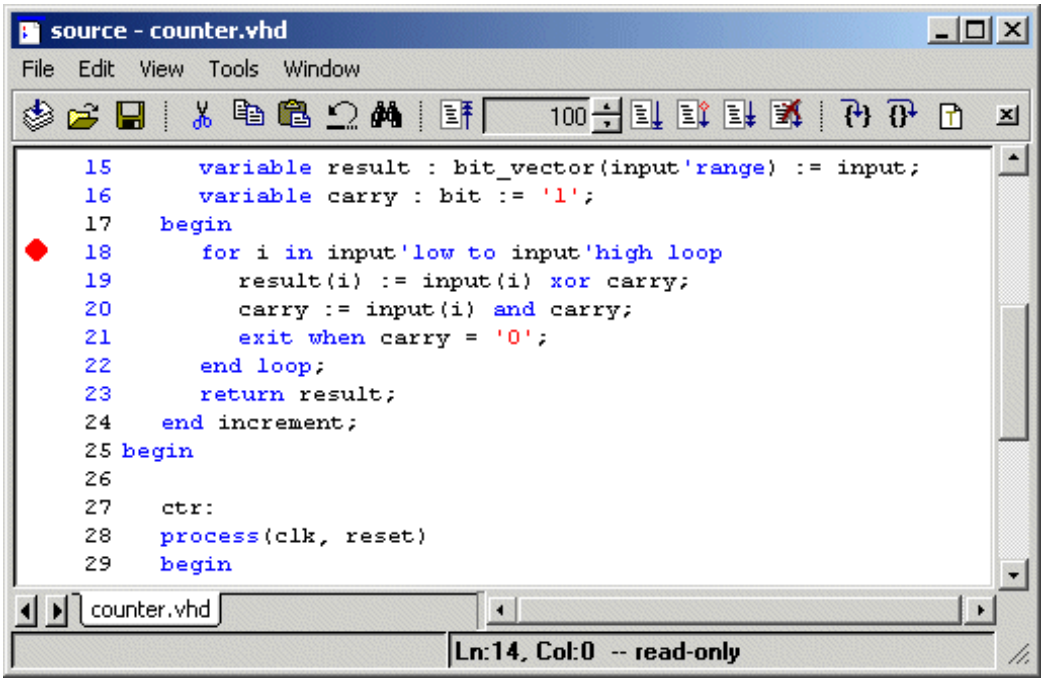
(Main MENU: Simulate > Break)

The arrow in the Source window points to the next HDL statement to be executed. (If the simulator is not evaluating a process at the time the Break occurs, no arrow will be displayed in the Source window.)

4 Next, you will set a breakpoint in the function on line 18. Scroll the Source window until line 18 is visible. Click on or near line number 18 to set the breakpoint.

You should see a red dot next to the line number where the breakpoint is set. The breakpoint can be toggled between enabled and disabled by clicking it. When a breakpoint is disabled, the dot appears open. To delete the breakpoint, click the line number with your right mouse button and select Remove Breakpoint 18.

(PROMPT: bp counter.vhd 18)



Note: Breakpoints can be set only on executable lines — denoted by blue line numbers.

5 Select the **Continue Run** button to resume the run that you interrupted. ModelSim will hit the breakpoint, as shown by an arrow in the Source window and by a Break message in the Main window.

(PROMPT: run -continue) (MENU: Simulate > Run > Continue)

6 Click the **Step** button in the Main or Source window several times to single-step through the simulation. Notice that the values change in the Variables window (you may need to expand the Variables window).

(PROMPT: step) (MENU: Simulate > Run > Step)

7 This concludes the basic VHDL simulation tutorial. When you're done, quit the simulator by entering the command:

```
quit -force
```

This command exits ModelSim without asking for confirmation.

Lesson 3 - Basic Verilog simulation

The goals for this lesson are:

- Compile a Verilog design
- List signals in the design
- Examine the hierarchy of the design
- Simulate the design
- Change the default run length
- Set a breakpoint

The project feature covered in Lesson 1 executes several actions automatically such as creating and mapping work libraries. In this lesson we will go through the entire process so you get a feel for how ModelSim really works.

Compiling the design

If you've completed any previous VHDL lesson, you'll notice that Verilog and VHDL simulation processes are almost identical.

1. Create and change to a new directory to make it the current directory.

   You can make the directory current by invoking ModelSim from the new directory or by using the **File > Change Directory** command from the ModelSim Main window.

2. Copy the Verilog files (files with ".v" extension) from the *\<install_dir>\modeltech\examples* directory into the current directory.

   Before you can compile a Verilog design, you need to create a design library in the new directory. If you are familiar only with interpreted Verilog simulators such as Cadence Verilog-XL, this will be a new idea for you. Since ModelSim is a compiled Verilog simulator, it requires a target design library for the compilation. ModelSim can compile both VHDL and Verilog code into the same library if desired.

3. Invoke ModelSim:

   for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

   ```
   modelsim.exe
   ```

   Note: If you didn't add Model*Sim* to your search path during installation, you will have to include the full path when you type this command at a DOS prompt.

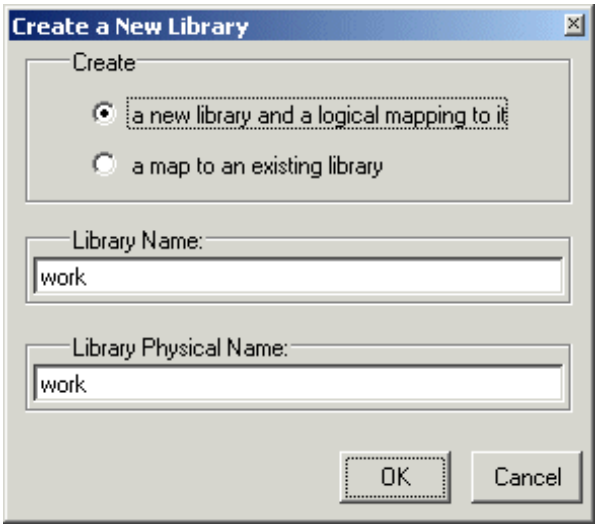
   Click **Close** if the Welcome dialog appears.

4 Before you compile any HDL code, you'll need a design library to hold the compilation results. To create a new design library, make this menu selection in the Main window: **File > New > Library**.

Make sure **Create: a new library and a logical mapping to it** is selected. Type "work" in the Library Name field and then select **OK**.

This creates a subdirectory named *work* - your design library - within the current directory. ModelSim saves a special file named *_info* in the subdirectory.

(PROMPT: vlib work
vmap work work)



Note: Do not create a Library directory using Windows commands, because the *_info* file will not be created. Always use the File menu or the **vlib** command from either the ModelSim or DOS prompt.)

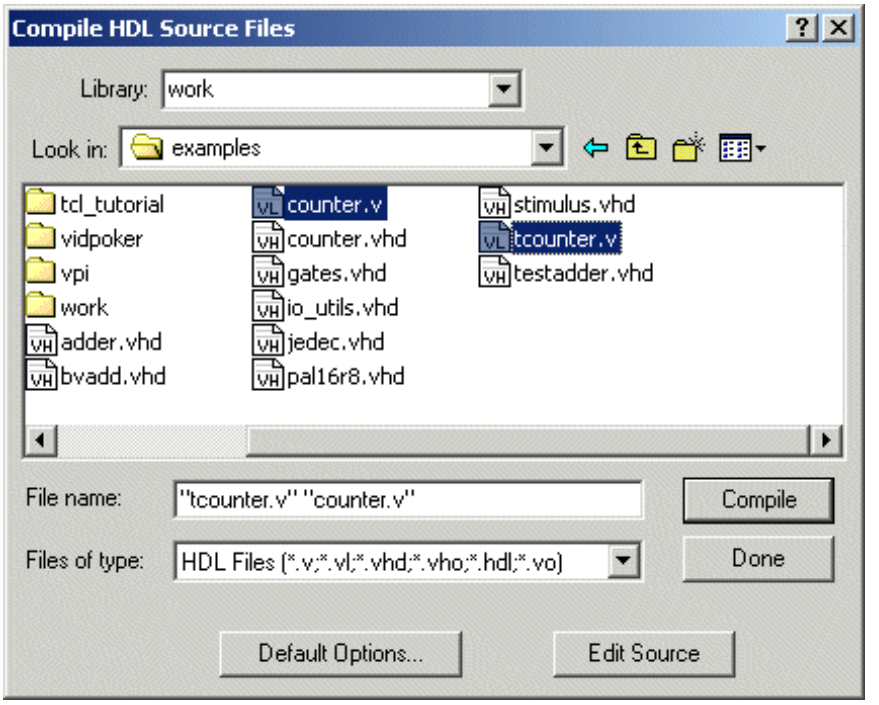
In the next step you'll compile the Verilog design. The example design consists of two Verilog source files, each containing a unique module. The file *counter.v* contains a module called **counter**, which implements a simple 8-bit binary up-counter. The other file, *tcounter.v*, is a testbench module (**test_counter**) used to verify **counter**.

Under simulation you will see that these two files are configured hierarchically with a single instance (instance name **dut**) of module **counter** instantiated by the testbench. You'll get a chance to look at the structure of this code later. For now, you need to compile both files into the **work** design library.

5 Compile the *counter.v*, and *tcounter.v* files into the **work** library by selecting **Compile > Compile** from the menu.

(PROMPT: vlog counter.v tcounter.v)

This opens the Compile HDL Source Files dialog box.



Select *counter.v* and *tcounter.v* (use Ctrl + click) and then choose **Compile** and then **Done**.

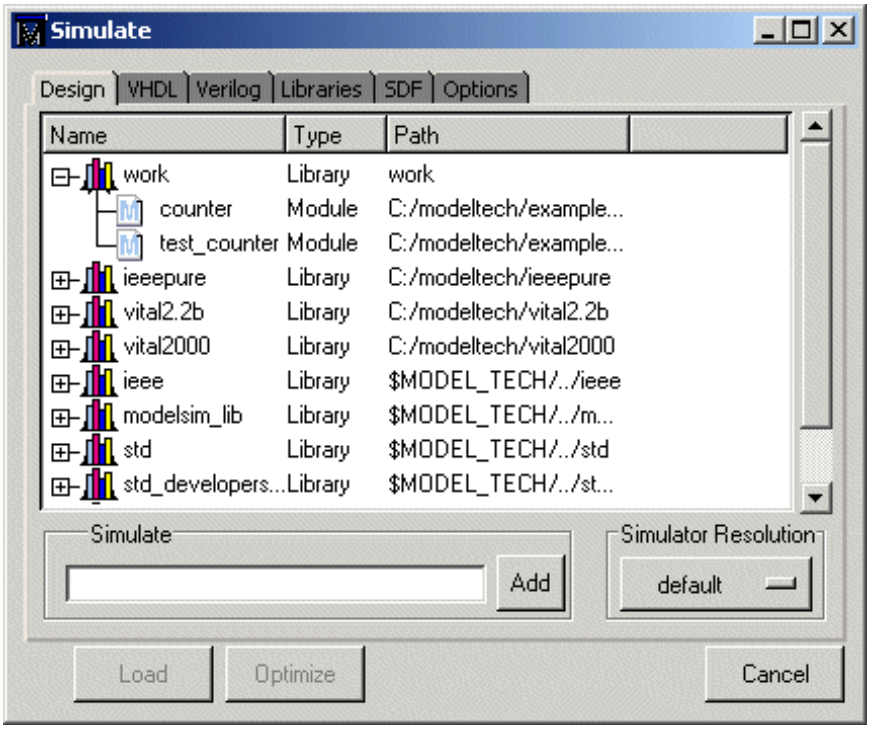
Note: The order in which you compile the two Verilog modules is not important (other than the source-code dependencies created by compiler directives). This may again seem strange to Verilog-XL users who understand the possible problems of interface checking between design units, or compiler directive inheritance. ModelSim defers such checks until the design is loaded. So it doesn't matter here if you choose to compile *counter.v* before or after *tcounter.v*.

Loading the design

1 Load the design by selecting **Simulate** > **Simulate** from the menu:

(PROMPT: vsim test_counter)

The Simulate dialog appears. Click the "+" sign next to 'work' to see the **counter** and **test_counter** design units. (You won't see this dialog box if you invoke **vsim** with *test_counter* from the command line.)



The Simulate dialog allows you to select a design unit to load from the specified library. You can also select the resolution limit for the simulation. The default resolution is 1 ns.

Select **test_counter** and click **Load** to accept these settings.

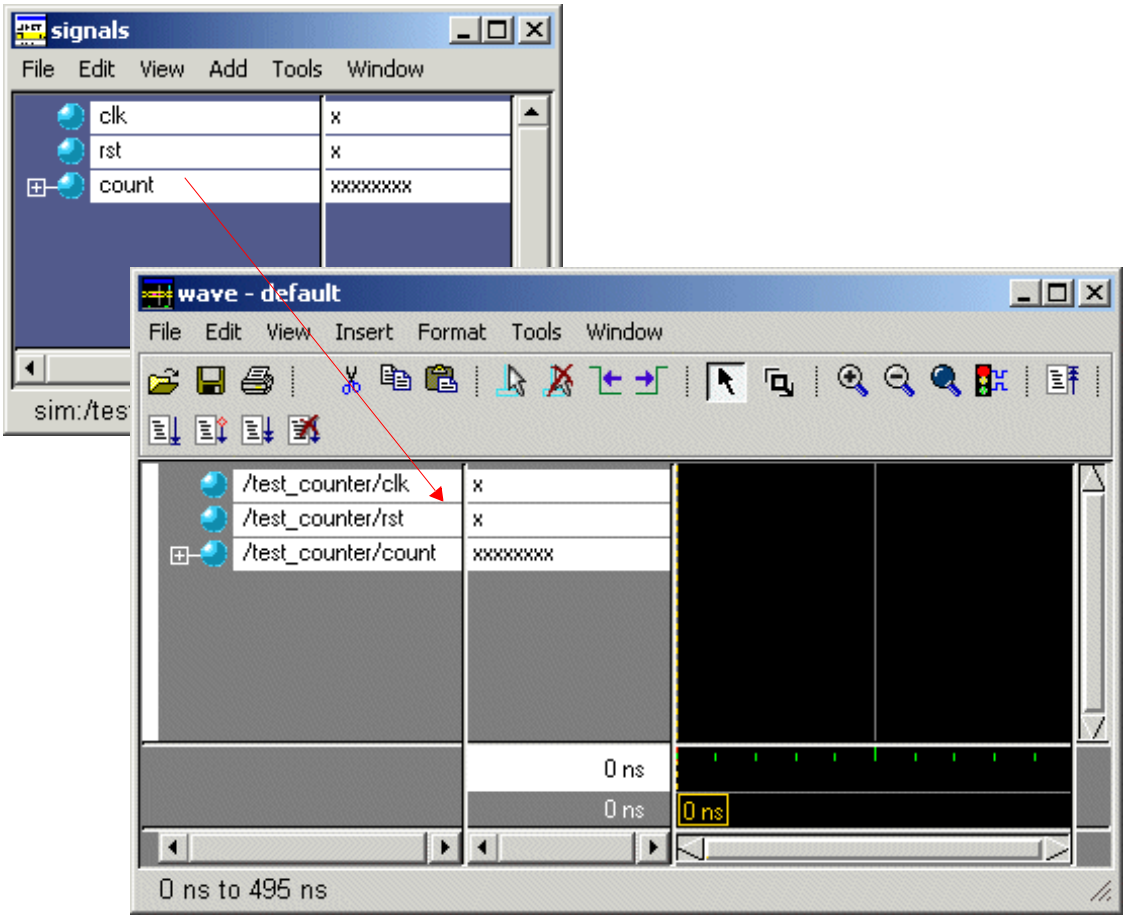
2 Bring up the Signals, Source, and Wave windows by entering the following command at the VSIM prompt within the Main window:

```
view signals source wave
```

(Main MENU: View > <window name>)

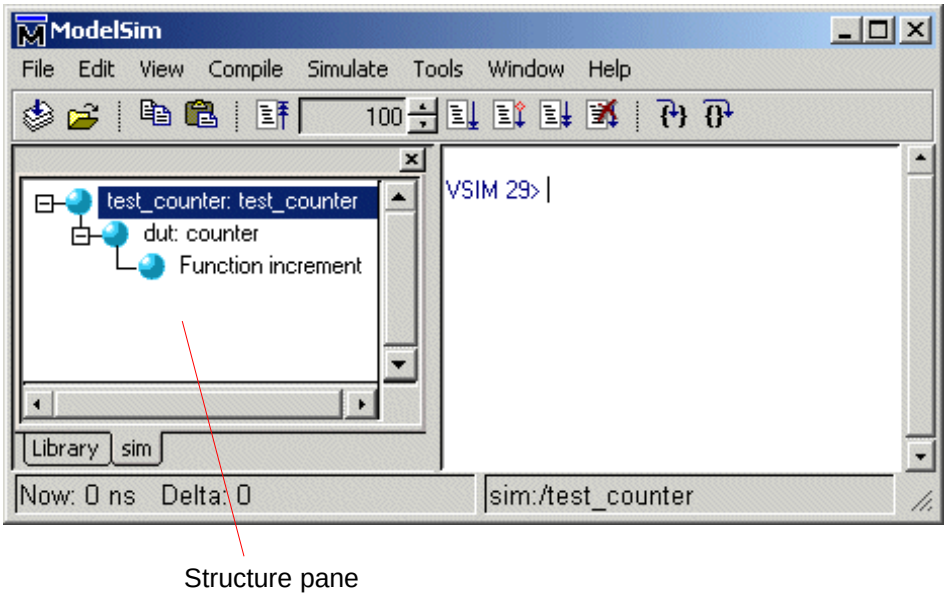
3 Now let's add signals to the Wave window with ModelSim's drag and drop feature.

In the Signals window, select **Edit > Select All** to select the three signals. Drag the signals to either the pathname or the values pane of the Wave window.



HDL items can also be copied from one window to another (or within the Wave and List windows) with the **Edit > Copy** and **Edit > Paste** menu selections.

4 You may have noticed when you loaded the design in Step 1 that a new tab appeared in the workspace area of the Main window.



The Structure tab shows the hierarchical structure of the design. By default, only the top level of the hierarchy is expanded. You can navigate within the hierarchy by clicking on any line with a "+" (expand) or "-" (contract) symbol. The same navigation technique works anywhere you find these symbols within ModelSim.

By clicking the "+" next to **dut: counter** you can see all three hierarchical levels: **test_counter**, **counter** and a function called **increment**. (If **test_counter** is not displayed you simulated **counter** instead of **test_counter**.)

5 Click on **Function increment** and notice how other ModelSim windows are automatically updated as appropriate. Specifically, the Source window displays the Verilog code at the hierarchical level you selected in the Structure window, and the Signals window displays the appropriate signals. Using the Structure tab in this way is analogous to scoping commands in interpreted Verilogs.

For now, make sure the **test_counter** module is showing in the Source window by clicking on the top line in the Structure pane.

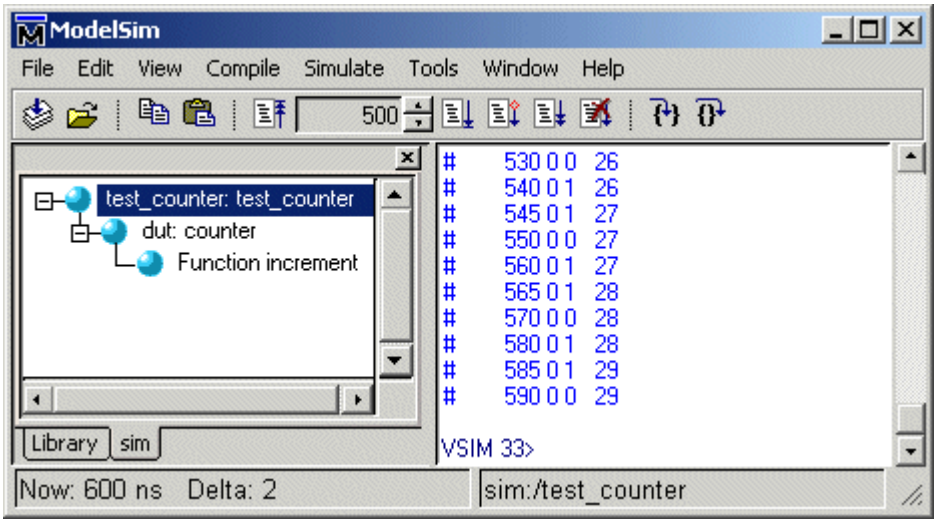
Running the simulation

Now you will exercise different Run functions from the toolbar.

1 Select the **Run** button on the Main window toolbar. This causes the simulation to run and then stop after 100 ns (the default simulation length).

(PROMPT: run) (MENU: Simulate > Run > Run 100 ns)

2 Next change the run length to 500 on the **Run Length** selector and select the **Run** button again.



Now the simulation has run for a total of 600ns (the default 100ns plus the 500 you just asked for). The status bar at the bottom of the Main window displays this information.

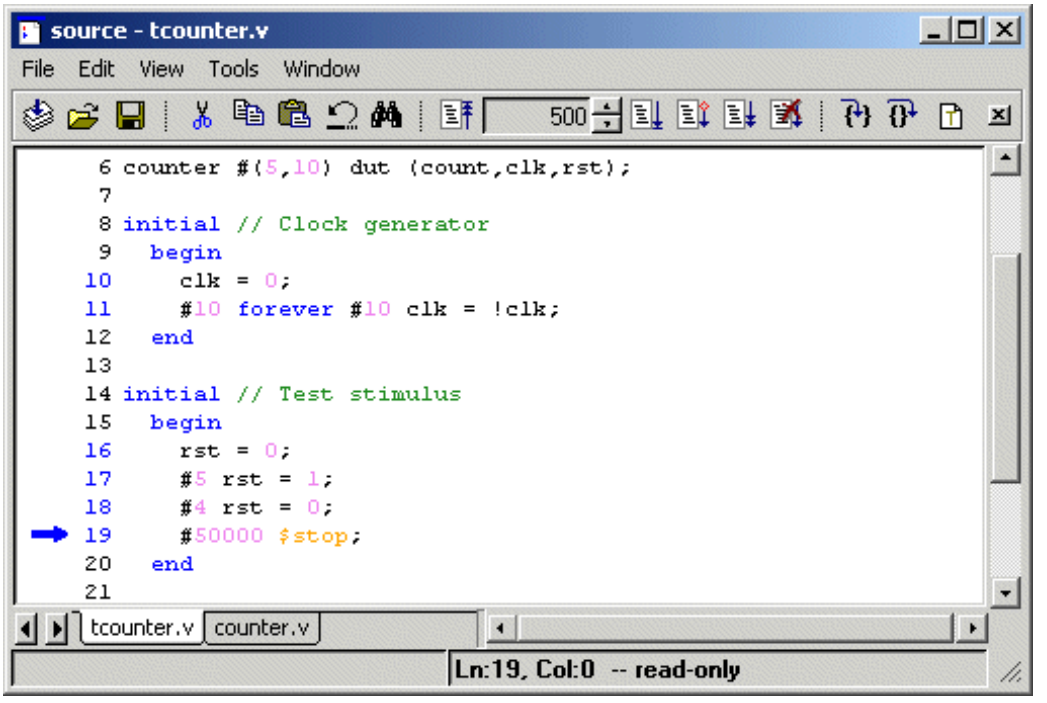
3 The last command you executed (**run 500**) caused the simulation to advance for 500ns. You can also advance simulation to a specific time. Type:

```
run @ 3000
```

This advances the simulation to time 3000ns. Note that the simulation actually ran for an additional 2400ns (3000 - 600).

4 Now select the **Run -All** button from the Main window toolbar. This causes the simulator to run until the stop statement in *tcounter.v*.

(PROMPT: run -all) (MENU: Simulate > Run > Run -All)



You can also use the **Break** button to interrupt a run.

(MENU: Simulate > Break)

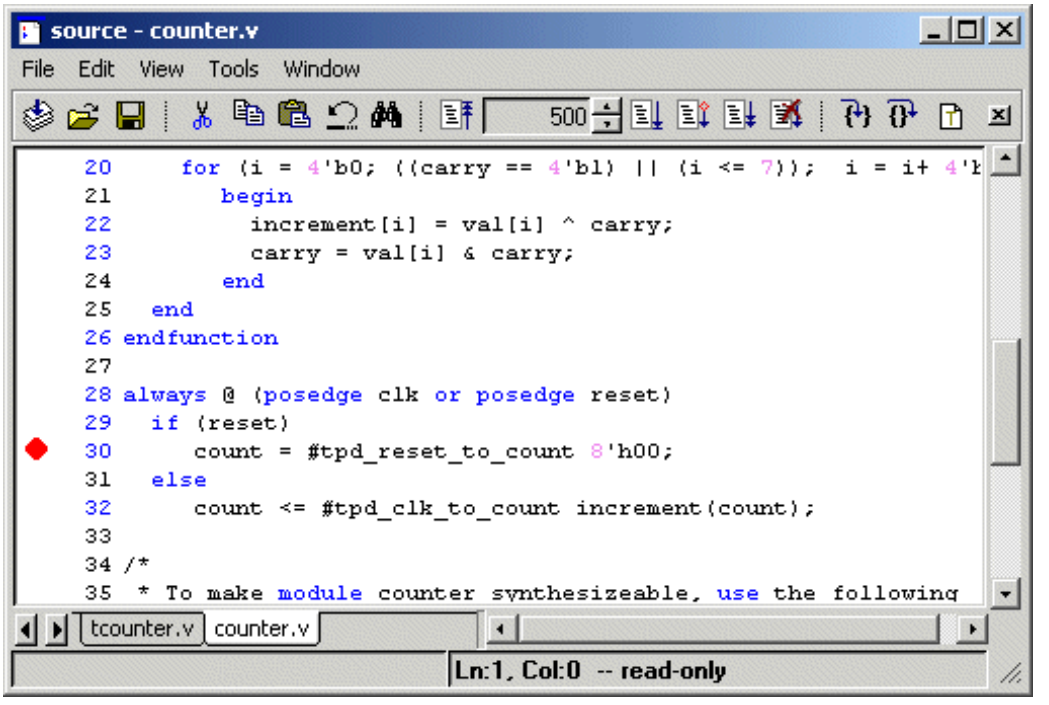
Debugging

Next we'll take a brief look at an interactive debugging feature of the ModelSim environment.

1 Let's set a breakpoint at line 30 in the *counter.v* file (which contains a call to the Verilog function increment). To do this, select **dut: counter** in the Structure pane of the Workspace. Move the cursor to the Source window and scroll the window to display line 30. Click on or near line number 30 to set a breakpoint. You should see a red dot next to the line number where the breakpoint is set.

The breakpoint can be toggled between enabled and disabled by clicking it. When a breakpoint is disabled, the dot appears open. To delete the breakpoint, click the line number with your right mouse button and select Remove Breakpoint.

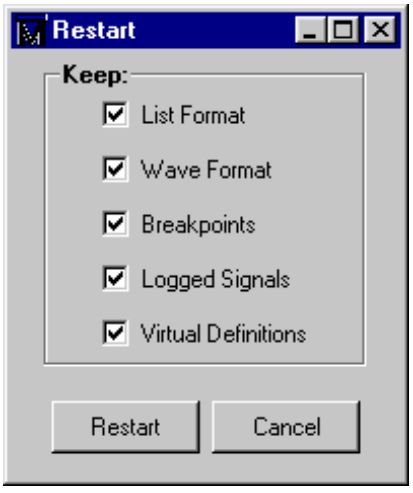
Note: Breakpoints can be set only on executable lines — denoted by blue line numbers.



2 Select the **Restart** button to reload the design elements and reset the simulation time to zero.

(Main MENU: Simulate > Run > Restart) (PROMPT: restart)

Make sure all items in the Restart dialog box are selected, then click **Restart**.



3 Select the **Run -All** button to re-start the simulation run.

(PROMPT: run -all) (Main MENU: Simulate > Run > Run -All)

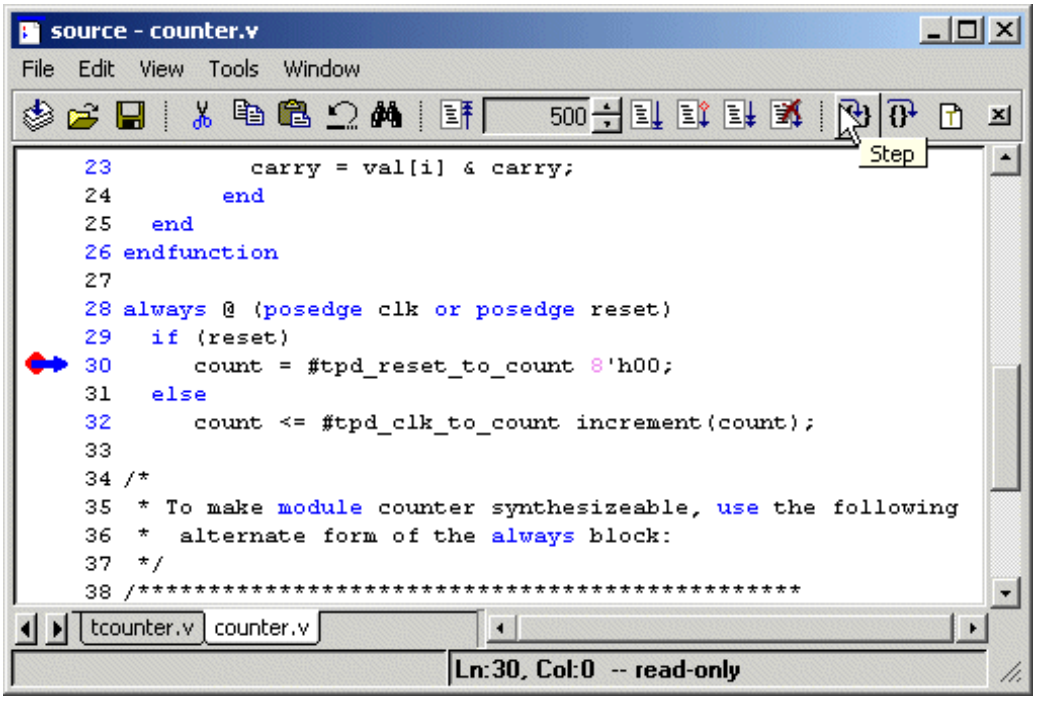
When the simulation hits the breakpoint, it stops running, highlights the line with an arrow in the Source window, and issues a Break message in the Main window.

4 When a breakpoint is reached, typically you will want to know one or more signal values. You have several options for checking values:

- look at the values shown in the Signals window
- hover your mouse pointer over the *count* variable in the Source window and a "balloon" will pop up with the value
- select the *count* variable in the Source window, right-click it, and select Examine from the context menu;
- use the **examine** command to output the value to the Main window transcript:

```
examine count
```

5 Let's move through the Verilog source functions with ModelSim's Step command. Click **Step** on the toolbar.



This command single-steps the debugger.

6 Experiment by yourself for awhile. Set and clear breakpoints and use the Step and Step Over commands until you feel comfortable with their operation. When you're done, quit the simulator by entering the command:

```
quit -force
```

Lesson 4 - Mixed VHDL/Verilog simulation

The goals for this lesson are:

- Compile multiple VHDL and Verilog files
- Simulate a mixed VHDL and Verilog design
- View the design in the Structure window
- View the HDL source code in the Source window

Note: You must be using ModelSim PE/PLUS to do this lesson.

Compile the design

1 Start by creating a new directory for this exercise. Create the directory, then copy the VHDL and Verilog example files to the directory:

```
<install_dir>\modeltech\examples\mixedHDL\*.vhd
<install_dir>\modeltech\examples\mixedHDL\*.v
```

Make sure the new directory is the current directory. Do this by invoking ModelSim from the new directory or by using the **File > Change Directory** command from the ModelSim Main window.

2 Start ModelSim with one of the following:

for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

```
modelsim.exe
```

Note: If you didn't add ModelSim to your search path during installation, you will have to include the full path when you type this command at a DOS prompt.

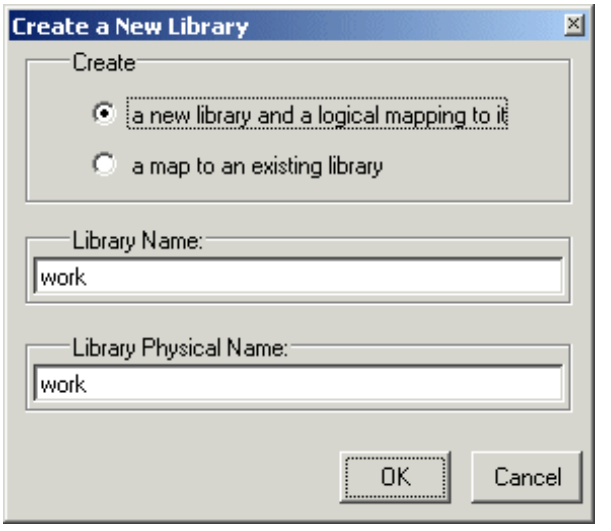
Select "Proceed to ModelSim" if the Welcome dialog appears.

3 Before you compile any HDL code, you'll need a design library to hold the compilation results. To create a new design library, make this menu selection in the Main window: **File > New > Library**.

Make sure **Create: a new library and a logical mapping to it** is selected. Type "work" in the Library Name field and then select **OK**.

This creates a subdirectory named *work* - your design library - within the current directory. ModelSim saves a special file named *_info* in the subdirectory.

(PROMPT: vlib work
vmap work work)

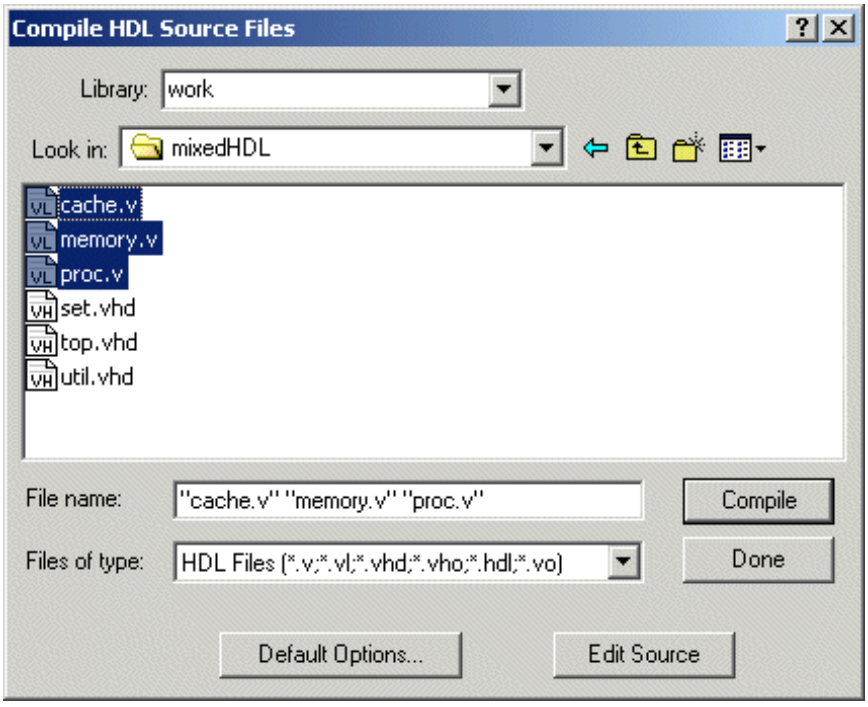


Note: Do not create a Library directory using Windows commands, because the *_info* file will not be created. Always use the File menu or the **vlib** command from either the ModelSim or DOS prompt.)

4 Compile the HDL files by selecting **Compile** > **Compile** from the menu:

(PROMPT: vlog cache.v memory.v proc.v)
(PROMPT: vcom util.vhd set.vhd top.vhd)

This opens the Compile HDL Source Files dialog box.



A group of Verilog files may be compiled in any order. However, in a mixed VHDL/Verilog design the Verilog files must be compiled before the VHDL files.

Compile the Verilog source by double-clicking each of these Verilog files in the file list (this invokes the Verilog compiler, **vlog**):

- *cache.v*
- *memory.v*
- *proc.v*

5. Depending on the design, the compile order of VHDL files can be very specific. In the case of this lesson, the file *top.vhd* must be compiled last.

   Stay in the Compile HDL Source Files dialog box and compile the VHDL files in this order (this invokes the VHDL compiler, **vcom**):

   - *util.vhd*
   - *set.vhd*
   - *top.vhd*

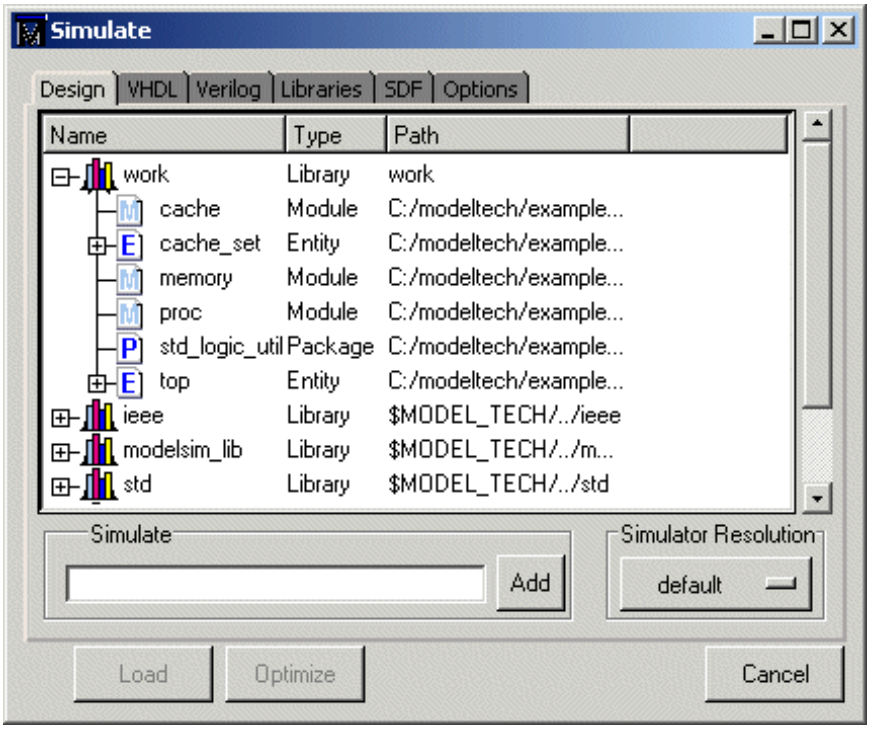
6. Click **Done** to dismiss the dialog box.

Loading the design

1 Load the design by selecting **Simulate > Simulate** from the menu.

(PROMPT: vsim top)

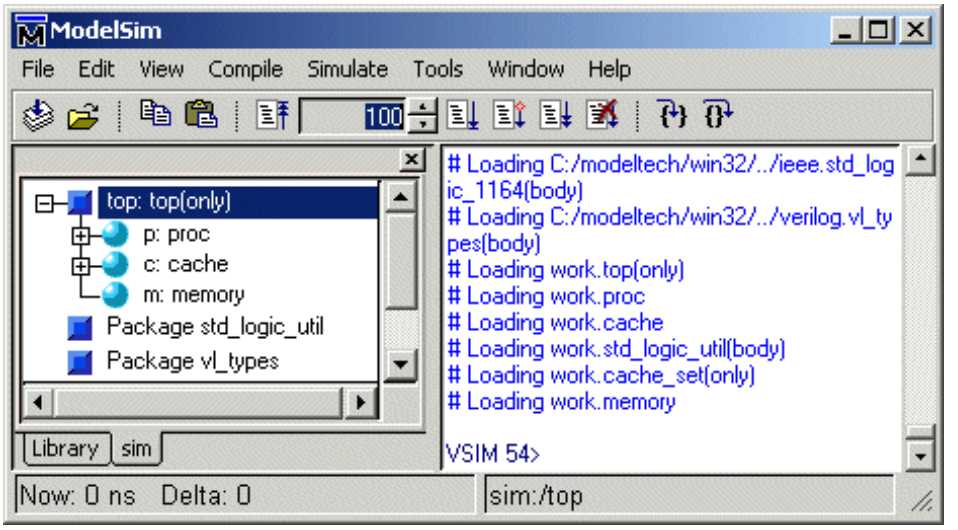
The Simulate dialog appears. Click the "+" sign next to 'work' to see the design units. (You won't see this dialog box if you invoke **vsim** with *top* from the command line.) Select **top** and then click **Load**.



2 From the Main menu select **View > All Windows** to open all ModelSim windows.

(PROMPT: view *)

3 Take a look at the Structure pane in the workspace.



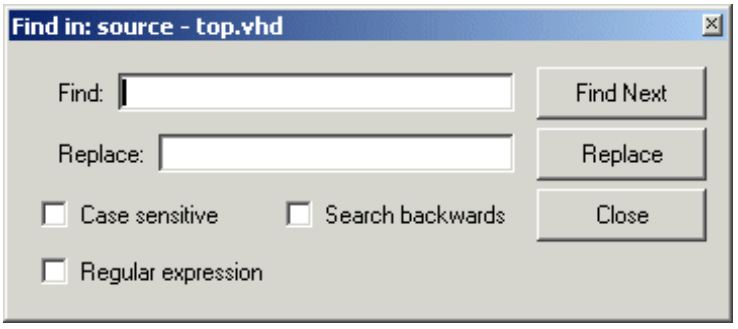
Notice the hierarchical mixture of VHDL and Verilog in the design. VHDL levels are indicated by a square “prefix”, while Verilog levels are indicated by a circle “prefix.” Try expanding (+) and contracting (-) the structure layers. You’ll find Verilog modules that have been instantiated by VHDL architectures, and similar instantiations of VHDL items by Verilog.

4 In the Structure pane, click on the Verilog module **c: cache**. The source code for the Verilog module is now shown in the Source window.

5 We'll use ModelSim's Find function to locate the declaration of cache_set within *cache.v*.

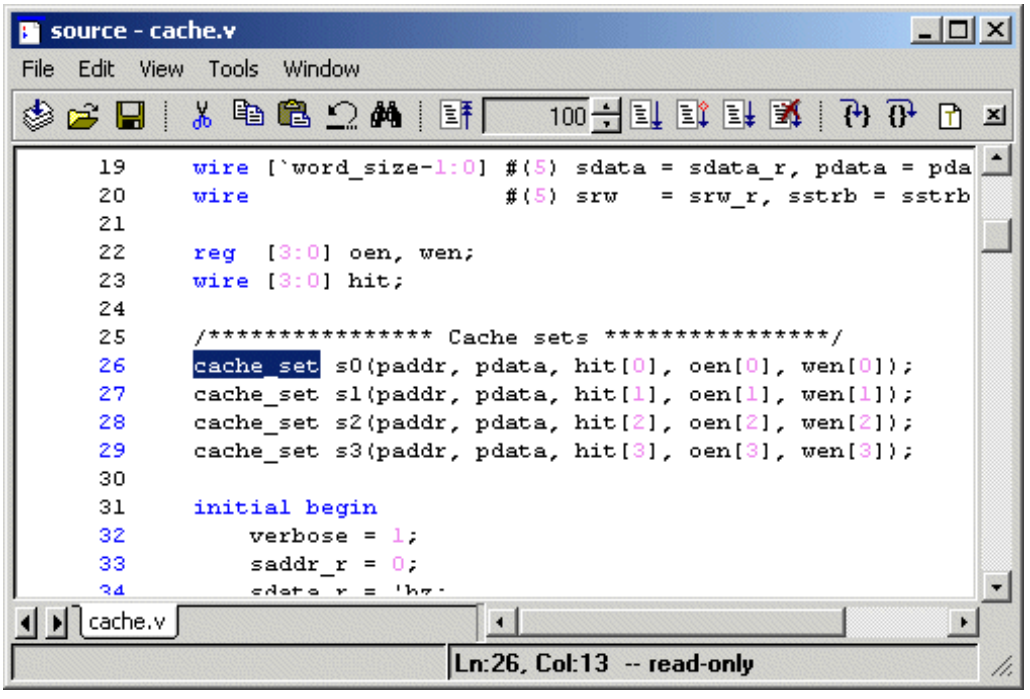
From the Source window menu select: **Edit > Find**:

The **Find in** dialog box is displayed.

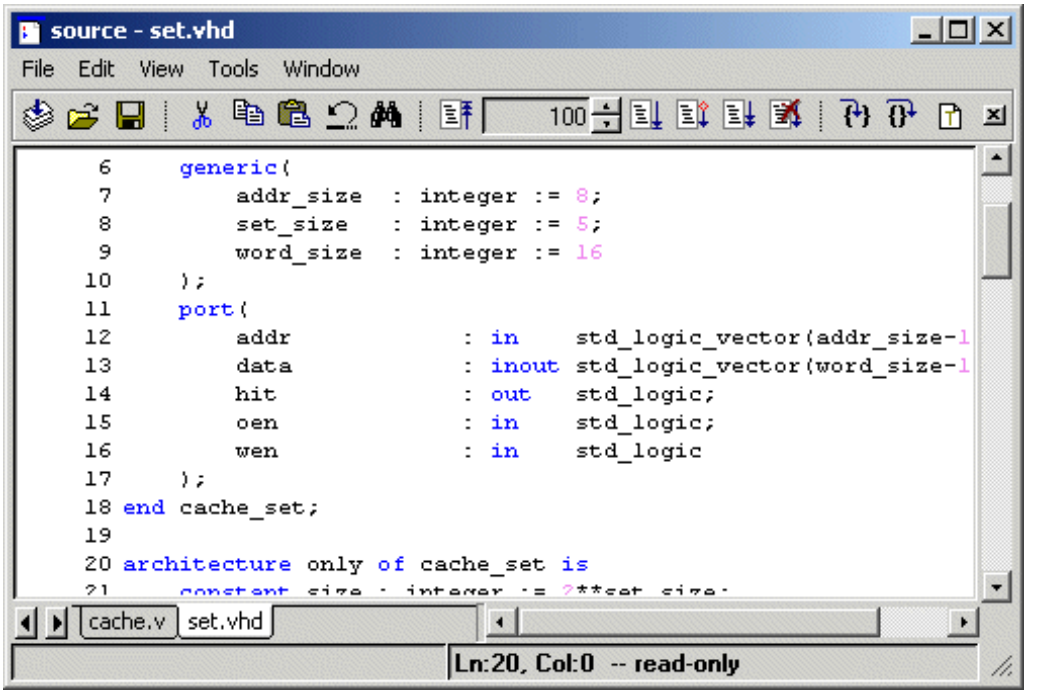


In the **Find:** field, type **cache_set** and click **Find Next**. The cache_set instantiations are now displayed in the Source window. (Click **Close** to dismiss the **Find in:** dialog box.)

Note that cache_set is a VHDL entity instantiated within the Verilog file *cache.v*.



6 Go back to the Main window, expand the **c:cache** entry by clicking the "+" sign, and scroll down and click on the line **"s0: cache_set(only)"**. The Source window shows the VHDL code for the cache_set entity.



Before you quit, try experimenting with some of the commands you've learned from previous lessons – add signals to the Wave window, run the simulation, etc. Note that in this design, "clk" is already driven, so you won't need to use the **force** command.

7 When you're ready to quit simulating, enter the command:

```
quit -force
```

Lesson 5 - Debugging a VHDL design

The goals for this lesson are:

- Map a logical library name to an actual library
- Change the default run length
- Recognize assertion messages in the Main window transcript
- Change the assertion break level
- Restart the simulation run using the **restart** command
- Examine composite types displayed in the Variables window
- Change the value of a variable

In this lesson we will debug an assertion message using the Source, Signals, and Variables windows. For another debugging lesson, see *Lesson 9 - Debugging with the Dataflow window*.

Compiling and loading the design

1. Create a new directory for this exercise and copy the following VHDL (.vhd) files from \<*install_dir*>*modeltech**examples* to the new directory.
   - gates.vhd
   - adder.vhd
   - testadder.vhd

2. Make sure the new directory is the current directory. Do this by invoking ModelSim from the new directory or by using the **File > Change Directory** command from the ModelSim Main window.

3. Start ModelSim with one of the following:

   for Windows - your option - from a Windows shortcut icon, from the Start menu, or from a DOS prompt:

   ```
   modelsim.exe
   ```

   Note: If you didn't add ModelSim to your search path during installation, you will have to include the full path when you type this command at a DOS prompt.

   Select "Proceed to ModelSim" if the Welcome dialog appears.

4. Enter the following command at the ModelSim prompt to create a new library:

   ```
   vlib library_2
   ```

5. Map the new library to the work library using the **vmap** command:

   ```
   vmap work library_2
   ```

   ModelSim adds this mapping to the *modelsim.ini* file.

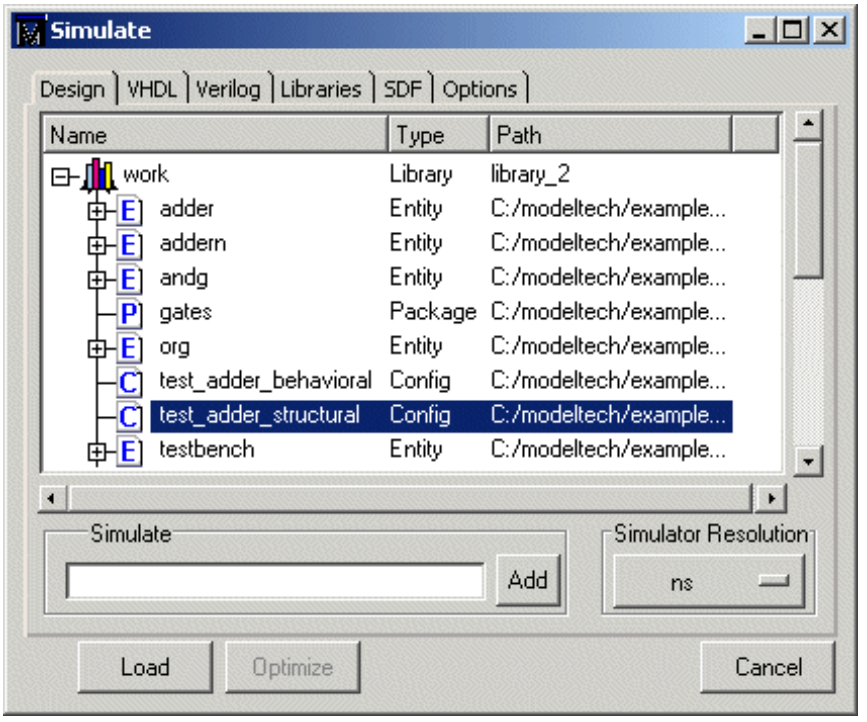
6. Compile the source files into the new library by entering this command at the ModelSim prompt:

   ```
   vcom -work library_2 gates.vhd adder.vhd testadder.vhd
   ```

7 Open the Simulate dialog by selecting **Simulate > Simulate**. Expand the work library and increase the width of the name column by clicking and dragging on the border between the Name and Type columns.

8 Make sure Simulator Resolution is set to nanoseconds, select **test_adder_structural**, and then click **Load**.

(PROMPT: vsim -t ns work.test_adder_structural)



Running the simulation

1. Start by opening the Variables and Signals windows using the command below. Note that you can abbreviate window names.

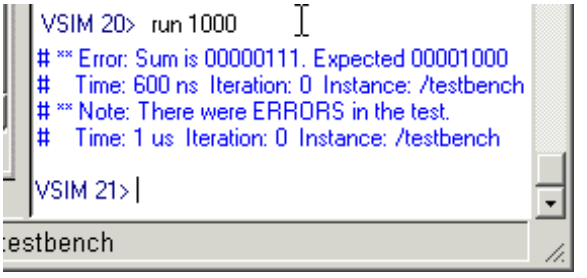
   ```
   view v si
   ```

   (Main MENU: View > <window name>)

2. Now run the simulation for 1000 ns:

   ```
   run 1000
   ```

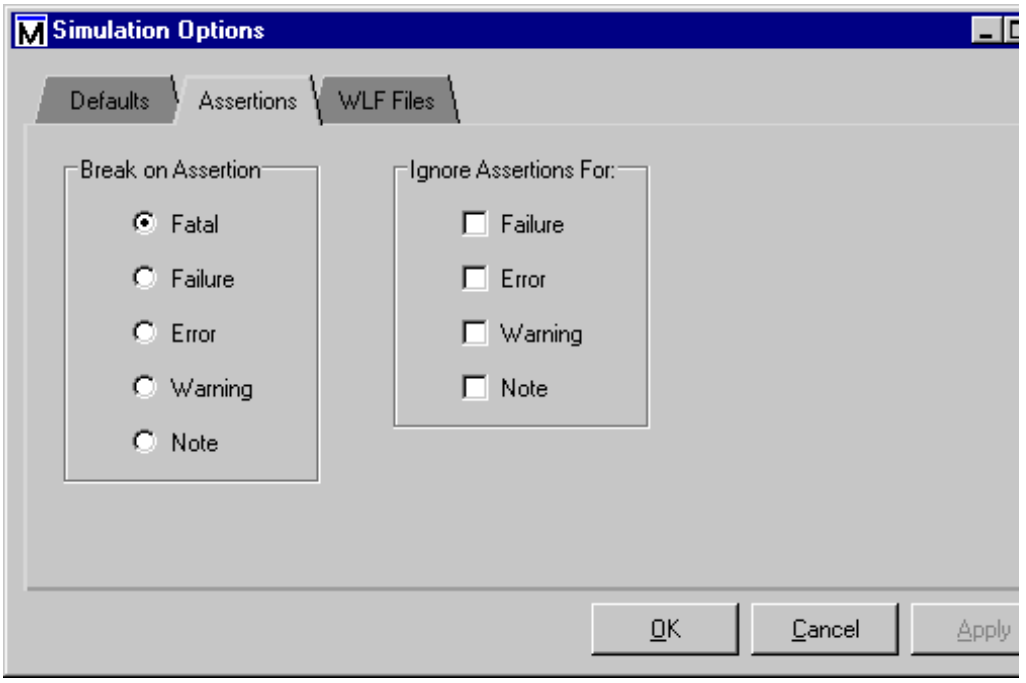
   A message in the Main window will notify you that there was an assertion error.



Debugging the simulation

Let's find out what's wrong. Perform the following steps to track down the assertion message.

1 First, change the simulation assertion options. Select **Simulate > Simulation Options** from the Main window menu.



2 Select the **Assertions** tab. Change the selection for **Break on Assertion** to **Error** and click **OK**. This will cause the simulator to stop at the HDL assertion statement.

3 Restart the simulation using the following command:

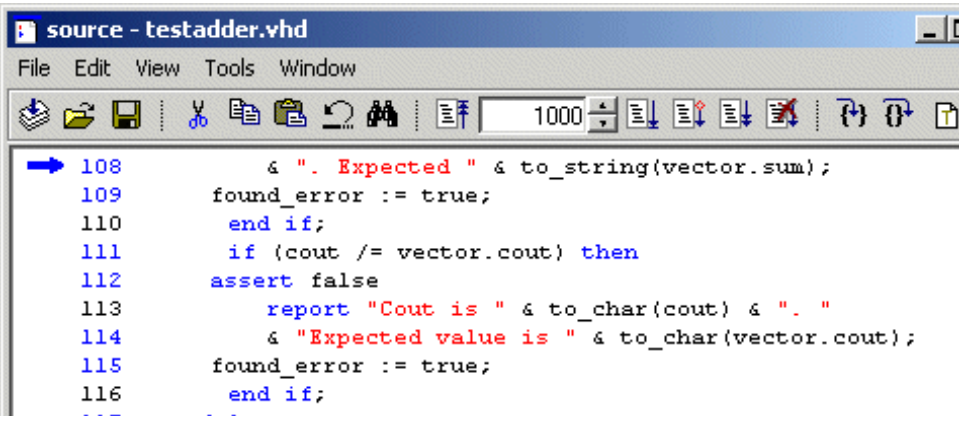
```
restart -f
```

The **-f** option causes ModelSim to restart without popping up the confirmation dialog.

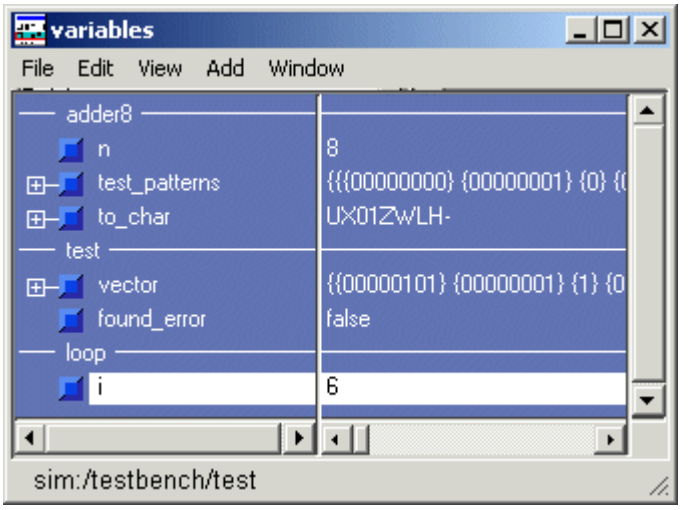
4 Run the simulation again for 1000 ns.

```
run 1000
```

Notice that the arrow in the Source window is pointing to the assertion statement.



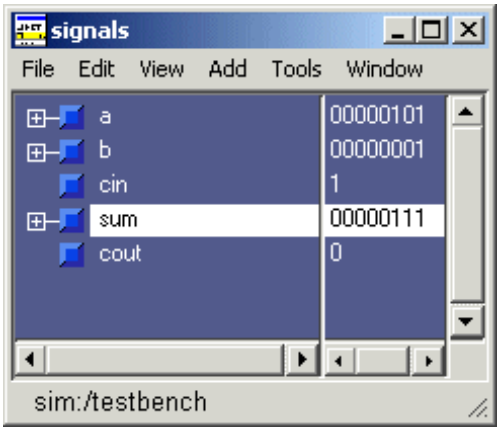
5 If you look at the Variables window now, you can see that i = 6. This indicates that the simulation stopped in the sixth iteration of the test pattern's loop.

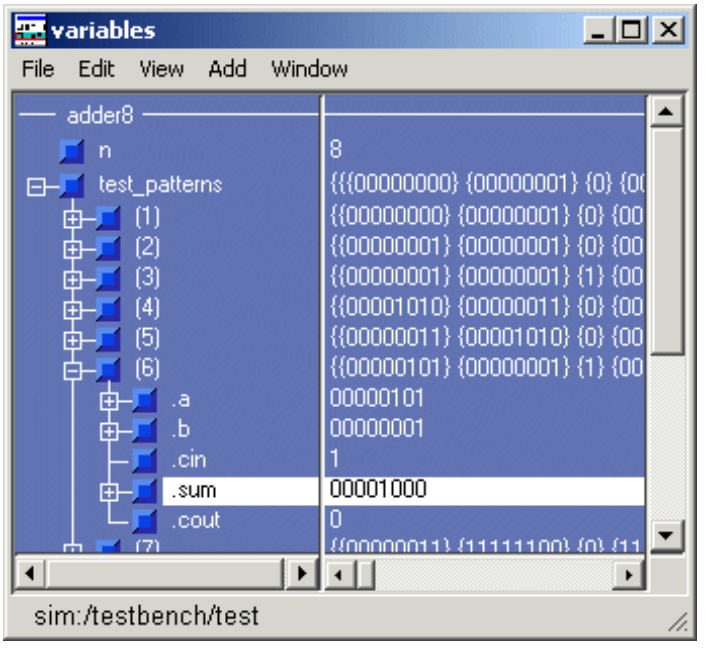


6 Expand the variable named **test_patterns** by clicking the [+]. (You may need to resize the window for a better view.)

7 Also expand the sixth record in the array **test_patterns(6)**, by clicking the [+]. The Variables window should be similar to the one below.

The assertion shows that the Signal **sum** does not equal the **sum** field in the Variables window. Note that the sum of the inputs **a**, **b**, and **cin** should be equal to the output **sum**. But there is an error in the test vectors. To correct this error, you need to restart the simulation and modify the initial value of the test vectors.



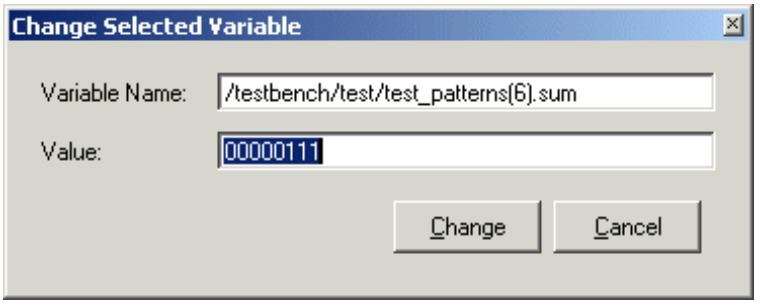


8 Restart the simulation again:

```
restart -f
```

9 Update the Variables window by selecting the **test** process in the Process window.

10 In the Variables window, expand **test_patterns** and **test_pattern(6)** again. Then highlight the **.sum** record by clicking on the variable name (not the box before the name) and select **Edit > Change** from the menu.

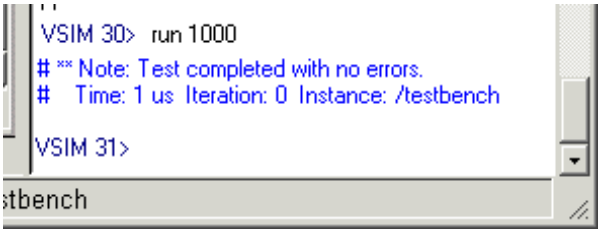


11 Change the value to **00000111** and then click **Change**. (Note that this is a temporary edit, you must use your text editor to permanently change the source code.)

12 Run the simulation again for 1000 ns.

```
run 1000
```

At this point, the simulation will run without errors.



This brings you to the end of this lesson, but feel free to explore the system further. When you are ready to end the simulation session, quit ModelSim by entering the following command at the VSIM prompt:

```
quit -f
```

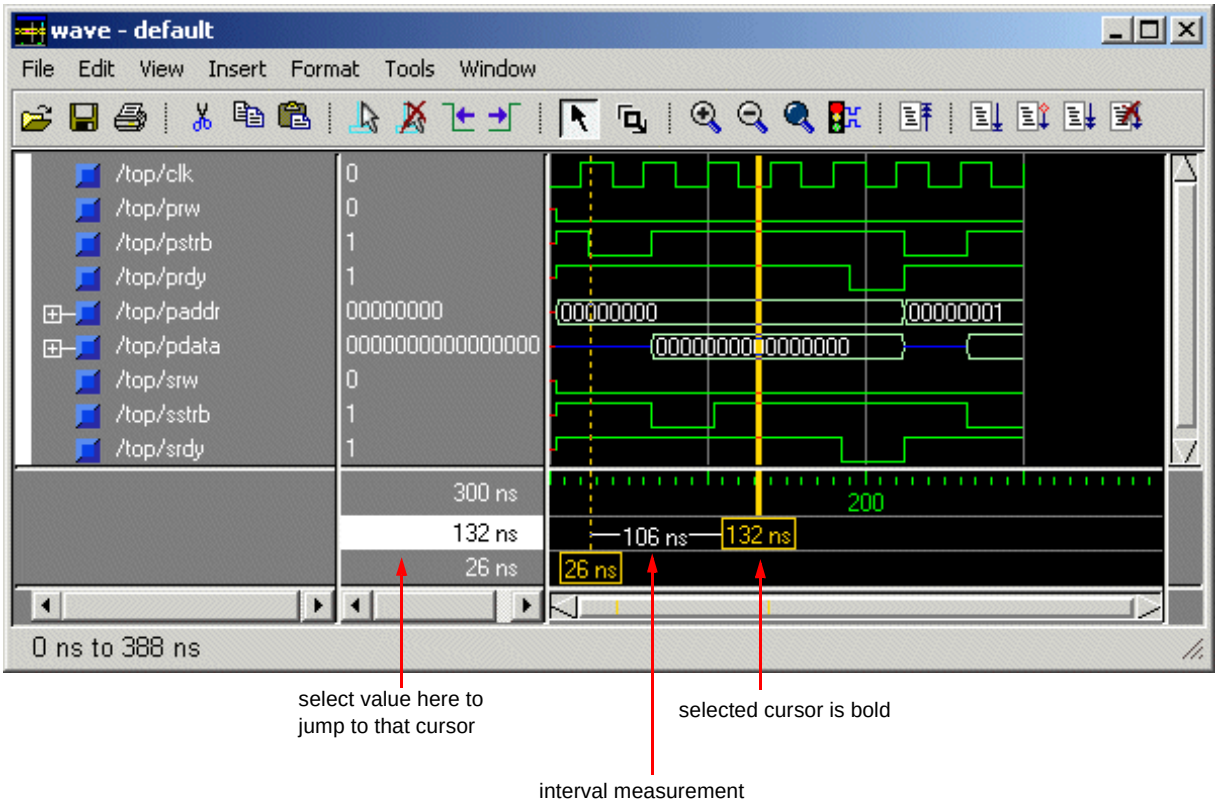
Lesson 6 - Using the Wave window

The goals for this lesson are:

- Practice using the Wave window time cursors.
- Practice zooming the waveform display.
- Practice using Wave window keyboard shortcuts.
- Practice combining items into a virtual object.
- Practice creating and viewing datasets.

Using time cursors in the Wave window

Any of the previous lesson simulations may be used with this part of the lesson, or use your own simulation if you wish.

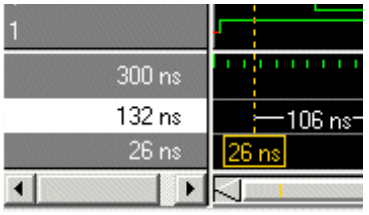


When the Wave window is first drawn, there is one cursor located at time zero. Clicking anywhere in the waveform display brings that cursor to the mouse location. You can add cursors to the waveform pane by selecting **Insert > Cursor** (or the Add Cursor button shown below). The selected cursor is drawn as a bold solid line; all other cursors are drawn with thin dashed lines. Remove cursors by selecting them and selecting **Edit > Delete Cursor** (or the Delete Cursor button shown below).

Add Cursor add a cursor to the Wave window	**Delete Cursor** delete the selected cursor from the window

Finding a cursor

The cursor value corresponds to the simulation time of that cursor. Choose a specific cursor view by selecting **View > Cursors** (Wave window). You can also select and scroll to a cursor by double-clicking its value in the cursor-value pane.



Alternatively, you can click a value with your second mouse button and type the value to which you want to scroll.

Making cursor measurements

Each cursor is displayed with a time box showing the precise simulation time at the bottom. When you have more than one cursor, each time box appears in a separate track at the bottom of the display. ModelSim also adds a delta measurement showing the time difference between two adjacent cursor positions.

If you click in the waveform display, the cursor closest to the mouse position is selected and then moved to the mouse position. Another way to position multiple cursors is to use the mouse in the time box tracks at the bottom of the display. Clicking anywhere in a track selects that cursor and brings it to the mouse position.

The cursors are designed to snap to the closest wave edge to the left on the waveform that the mouse pointer is positioned over. You can set the snap distance in the Window Preferences dialog (select **Tools > Window Preferences**).

You can position a cursor without snapping by dragging in the area below the waveforms.

You can also move cursors to the next transition of a signal with these toolbar buttons:

 **Find Previous Transition** locate the previous signal value change for the selected signal	 **Find Next Transition** locate the next signal value change for the selected signal

Zooming - changing the waveform display range

Zooming lets you change the simulation range in the waveform pane. You can zoom using a context menu, toolbar buttons, mouse, or keyboard.

Using the Zoom menu

You can use the Wave window menu bar, or call up the context menu by clicking the right mouse button in the waveform pane.

The Zoom menu options include:

- **Zoom In**
  Zooms in by a factor of two, increasing the resolution and decreasing the visible range horizontally.
- **Zoom Out**
  Zooms out by a factor of two, decreasing the resolution and increasing the visible range horizontally.
- **Zoom Full**
  Redraws the display to show the entire simulation from time 0 to the current simulation time.
- **Zoom Last**
  Restores the display to where it was before the last zoom operation.
- **Zoom Range**
  Brings up a dialog box that allows you to enter the beginning and ending times for a range of time units to be displayed.

Zooming with toolbar buttons

These zoom buttons are available on the toolbar:

 **Zoom in 2x** zoom in by a factor of two from the current view	 **Zoom out 2x** zoom out by a factor of two from current view
 **Zoom Full** zoom out to view the full range of the simulation from time 0 to the current time	 **Zoom Mode** change mouse pointer to zoom mode; see below

Zooming with the mouse

To zoom with the mouse, first enter zoom mode by selecting **View > Mouse Mode > Zoom Mode** (Wave window). The left mouse button (<Button-1>) then offers 3 zoom options by clicking and dragging in different directions:

- Down-Right: Zoom Area (In)
- Up-Right: Zoom Out
- Up-Left: Zoom Fit

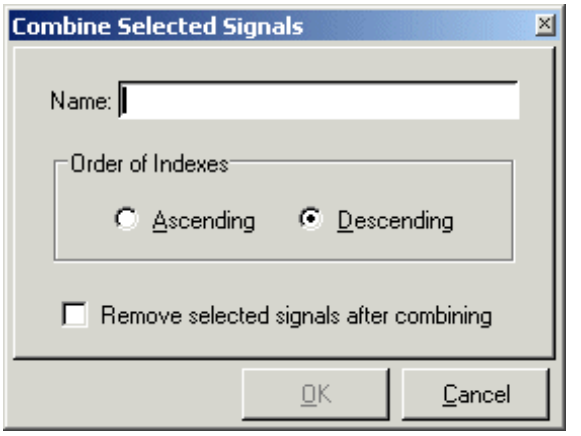
The zoom amount is displayed at the mouse cursor. A zoom operation must be more than 10 pixels to activate.

Keyboard shortcuts for zooming

Using the following keys when the mouse cursor is within the Wave window will cause the indicated actions:

Key	Action
i I or +	zoom in
o O or -	zoom out
f or F	zoom full
l or L	zoom last
r or R	zoom range
<arrow up>	scroll waveform display up
<arrow down>	scroll waveform display down
<arrow left>	scroll waveform display left
<arrow right>	scroll waveform display right
<page up>	scroll waveform display up by page
<page down>	scroll waveform display down by page
<tab>	searches forward (right) to the next transition on the selected signal
<shift-tab>	searches backward (left) to the previous transition on the selected signal
<Control-f>	opens the find dialog box; searches within the specified field in the pathname pane for text strings

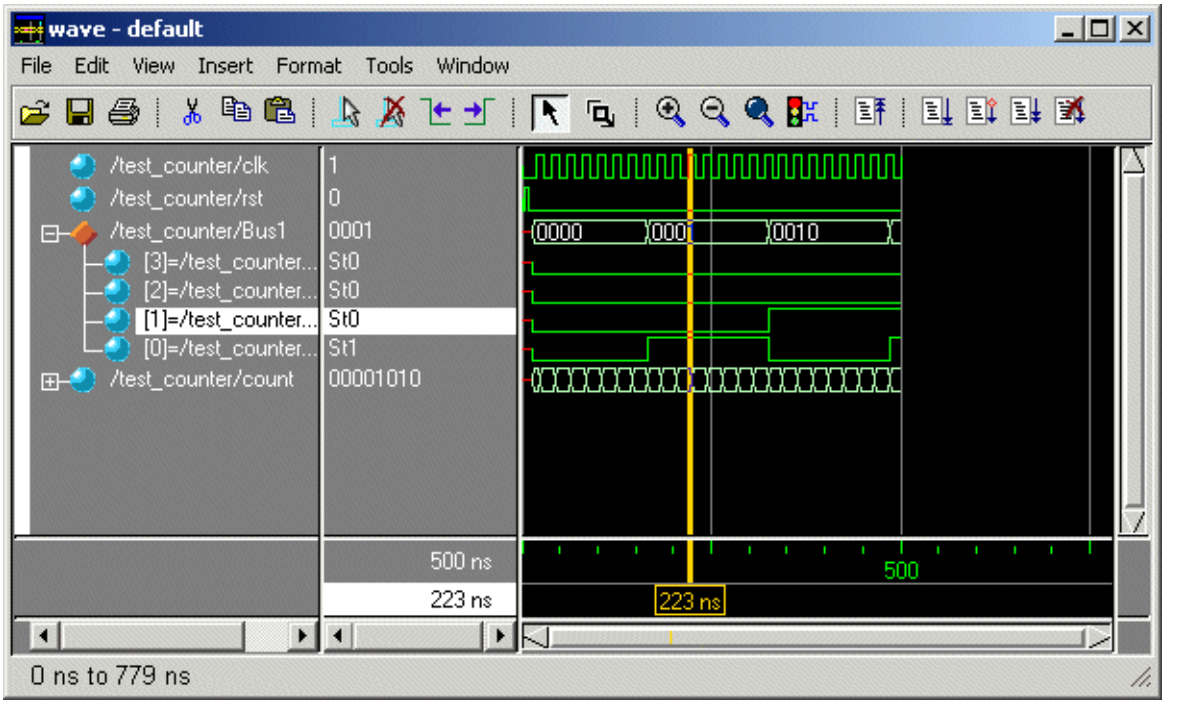
Combining items in the Wave window



The Wave window allows you to combine signals into buses. Select **Tools > Combine Signals** to open the Combine Selected Signals dialog.

A bus is a collection of signals concatenated in a specific order to create a new virtual signal with a specific value.

In the illustration below, three data signals have been combined to form a new bus called Bus1. Notice, the new bus has a value that is made up of the values of its component signals arranged in a specific order. Virtual objects are indicated by an orange diamond.



Creating and viewing datasets

Datasets allow you to view previous simulations or to compare simulations. To view a dataset, you must first save a ModelSim simulation to a WLF file (using the **vsim -wlf** command). Once you have saved a WLF file, you can open it as a view-mode dataset.

In this lesson you will compare two simple Verilog designs: a structural description and an RTL description of a 4-bit, binary counter. To begin, you will simulate the structural description and save it to a WLF file. Then you will simulate the RTL version. Finally, you will open the WLF file as a dataset and compare the two simulations in the Wave window.

Simulating the structural version

1. Start by creating a new working directory, making it the current directory, and copying the files from *\modeltech\examples\datasets* into it.

2. Use the **vlib** command to create a **work** library in the current directory.

   ```
   vlib work
   ```

   (MENU: File > New > Library)

3. Use the **vmap** command to map the work library to a physical directory. A *modelsim.ini* file will be written into the current directory.

   ```
   vmap work work
   ```

4. Compile the structural version of the counter.

   ```
   vlog cntr_struct.v
   ```

   (MENU: Compile > Compile)

5. Load the design and save the simulation to a WLF file named *struct.wlf*.

   ```
   vsim -wlf struct.wlf work.cntr_struct
   ```

6. Now you will run a DO file that applies stimulus to the design, runs the simulation, and adds waves to the Wave window. Feel free to open the DO file and look at its contents.

   ```
   do stimulus.do
   ```

   (MENU: Tools > Execute Macro)

   The waves that appear in the Wave window are saved automatically into the *struct.wlf* file.

7. Quit the simulation.

   ```
   quit -sim
   ```

   (MENU: Simulate > End Simulation)

Simulating the RTL version

1. Compile the RTL version of the counter.

   ```
   vlog cntr_rtl.v
   ```

2. Simulate the design.

   ```
   vsim work.cntr_rtl
   ```

   (MENU: Simulate > Simulate)

3. Run the DO file to apply stimulus to the design.

   ```
   do stimulus.do
   ```

Comparing the two designs

To compare the two simulations, we will create a second pane in the Wave window, open the *struct.wlf* file, and add the signals from the dataset to the new pane.

1. Add a second pane to the Wave window.

   Wave MENU: Insert > Window Pane

   Notice that a thick, white vertical bar at the left edge of the window indicates that the new pane is active.

2. Open *struct.wlf*.

   ```
   dataset open struct.wlf
   ```

   (Wave MENU: File > Open Dataset)

3. Add signals for the "struct" dataset.

   ```
   add wave *
   ```

   Notice that the pathname prefix for the signals you just added is the dataset name "struct". The pathname prefix for the active simulation is "sim".

   The results for each simulation should be the same. You can continue experimenting with the two simulations or quit the simulation.

   ```
   quit -sim
   ```

   (Main MENU: Simulate > End Simulation)

Lesson 7 - Simulating with Code Coverage

The goals for this lesson are:

- Run a simulation with Code Coverage ON and examine the coverage_summary window
- Save line coverage information to a text file
- Exclude lines and files from the coverage statistics
- Append results from a previous simulation run onto the next one

ModelSim Code Coverage allows you to identify which lines in your code are being covered by the testbench. It is non-intrusive (instrumented code is *not* required) and only minimally impacts simulation performance (<5%).

Note: The Code Coverage feature is available as an add-on to the PE version. Contact Model Technology sales for more information.

Running a simulation with Code Coverage

All commands are shown as entered on the ModelSim command line.

1. Start by creating a new working directory, making it the current directory, and copying the files from *\modeltech\examples\profiler* into it.

2. Use the **vlib** command to create a **work** library in the current directory.

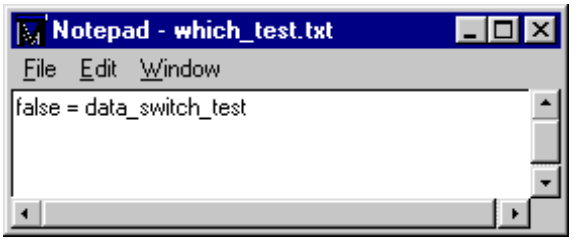
   ```
   vlib work
   ```

   (MENU: File > New > Library)

3. Use the **vmap** command to map the work library to a physical directory. A *modelsim.ini* file will be written into the **work** directory.

   ```
   vmap work work
   ```

4. Prior to running the simulation, we need to check the *which_test.txt* file in the *modeltech\examples\profiler* directory to ensure it reads "false = data_switch_test". You can edit the file with **notepad** within Model*Sim*.

   This switch configures the test bench – the *ringrtl.vhd* file. We'll change it later in the lesson when we merge the coverage results of two simulations.

5. Compile the lower level blocks of the design.

   ```
   vcom control.vhd retrieve_array.vhd store_array.vhd
   ```

   (MENU: Compile > Compile)

6. Compile the top level block, test bench, and configuration files.

   ```
   vcom ringrtl.vhd testring.vhd config_rtl.vhd
   ```

   (MENU: Compile > Compile)

7. Use the **vsim -coverage** command to load the design configuration with Code Coverage.

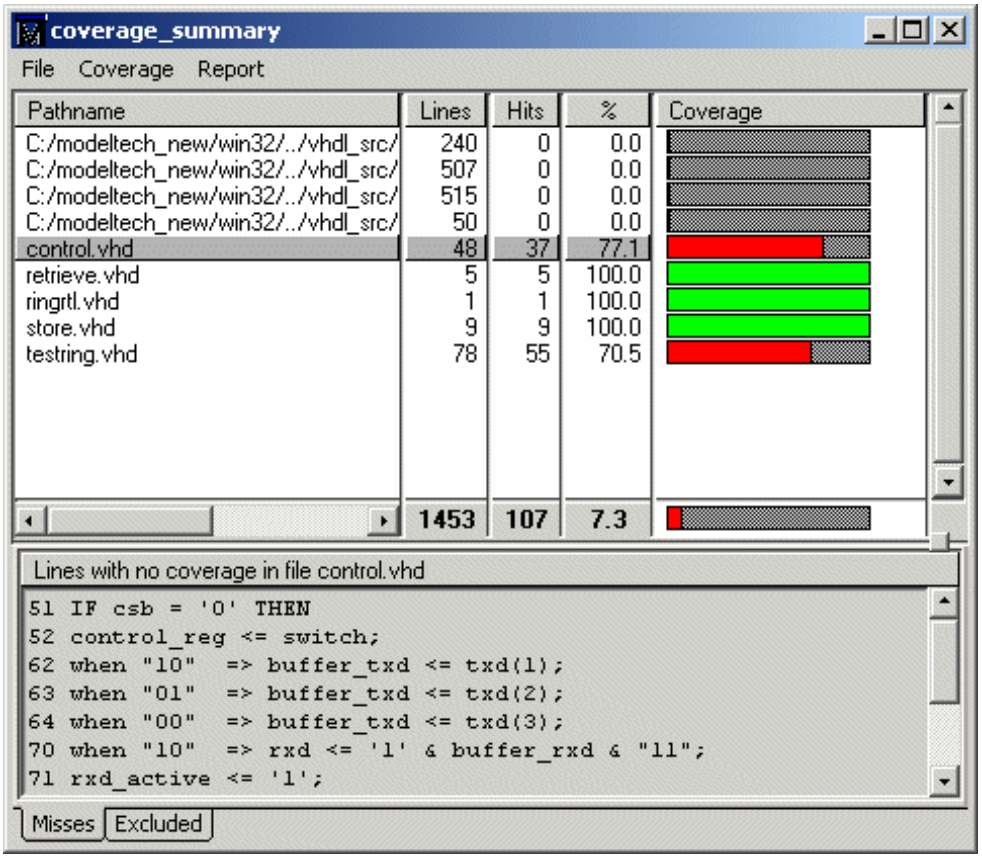
   ```
   vsim -coverage work.test_bench_rtl
   ```

8 Run the simulator for 3 milliseconds.

```
run 3 ms
```

9 Display the coverage_summary window.

```
view_coverage
```
(MENU: Tools > Source Coverage)

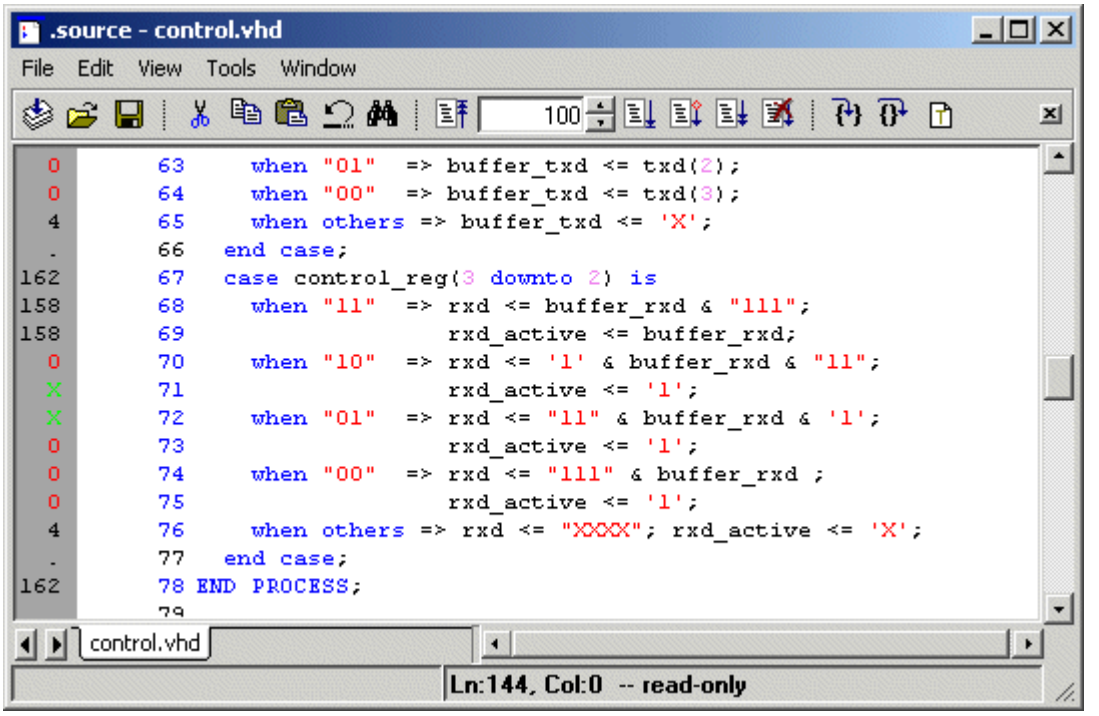


The top half of the window shows summary information on a per-file basis. If you select a file in the list, the bottom part of the window gives details about the lines in the file that have zero coverage.

Note that both *testring.vhd* and *control.vhd* are below 90% and, therefore, shown in red in the Coverage bar graph. 90% is the default coverage threshold, and all coverage values below 90% will be shown red. The default coverage threshold can be changed with the Tcl control variable *$PrefCoverage(cutoff)*.

10 Click on the *control.vhd* pathname to display the source code for *control.vhd* in the Source window. With Code Coverage enabled, the Source window is displayed with an extra column that details the number of times each line has been executed. The green "Xs" in the graphic below denote lines that have been excluded. We'll discuss that later in the lesson.

Scroll the Source window to view the executable lines. As you can see some lines have red zeros next to them. This indicates a line that was not executed.



11 Save the line coverage information to a text file.

```
coverage report -file cover.dat -lines
```
(coverage_summary MENU: Report > Save Line Coverage)

Open the file *cover.dat* to see how the data is stored. **Notepad** works well to check text files such as this.

```
notepad cover.dat
```

Excluding lines and files

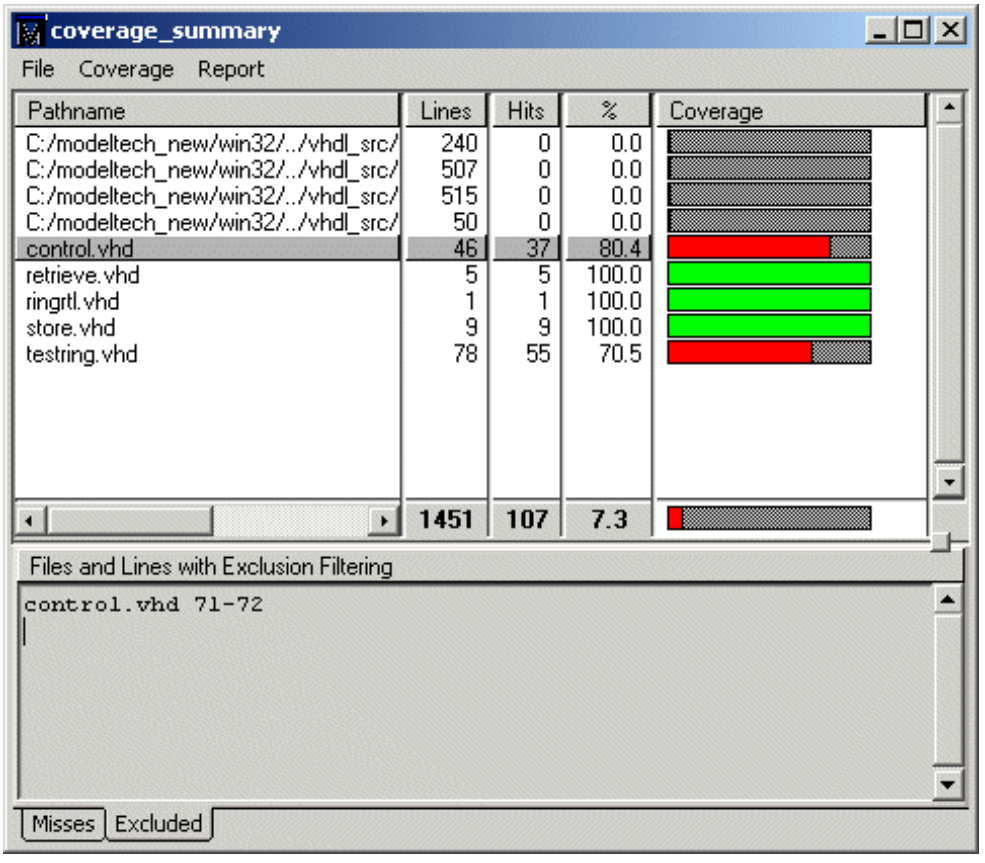
There may be a time when you want to exclude certain parts of your code from the analysis. You can exclude both lines and files from either the coverage_source or the coverage_summary windows.

1. Scroll to one of the executable lines in the Source window (noted with a blue line number).

2. With your mouse pointer over the column that shows coverage results (the left-most column), click your right-mouse button and select **Exclude Coverage Line #**.

3. The line will now be marked with a green "X" and the coverage statistics will be updated to exclude that line.

4. View the coverage_summary window and click the **Excluded** tab. This tab shows all the lines and files that are currently being excluded.



5 Select the line in the Excluded tab, click your right mouse button, and select **Include Entire Selected Files**. This removes the exclusion filter on any lines from the selected file.

You can continue experimenting with the various exclusion commands at this point if you want. However, before continuing with the tutorial, select **Coverage > Clear Out Current Filter** to ensure all lines and files are included for the next exercise.

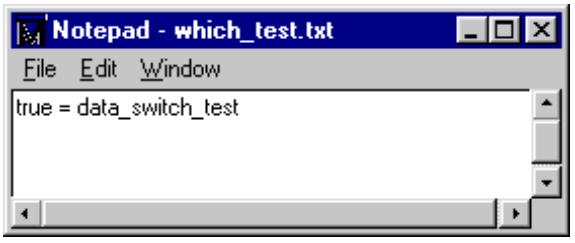
Merging coverage results from two simulations

You can merge code coverage results from multiple simulations. In this exercise, we'll change the test that is run by the test bench, resimulate, and then append the coverage statistics from our previous analysis to the new analysis.

1 Note how many times the clocked processes have been executed.

2 Next we'll edit the *which_test.txt* file. Changing this text file causes a different test to be run from the same test bench. Using ModelSim Notepad, edit the file so it reads "true = data_switch_test." Make sure the **Edit > read_only** switch is not on.

```
notepad which_test.txt
```



3 Restart the simulation so the different test is run on the circuit.

```
restart -f
```

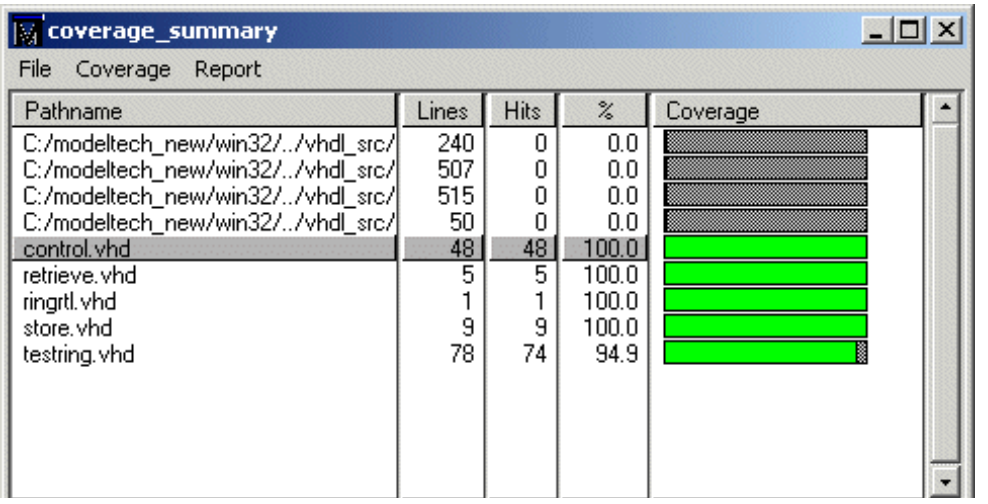
4 Restore the coverage data from the last simulation run so that its data can be appended to the current simulation.

```
coverage reload cover.dat
```
(coverage_summary MENU: File > Open > Coverage > Merge Coverage)

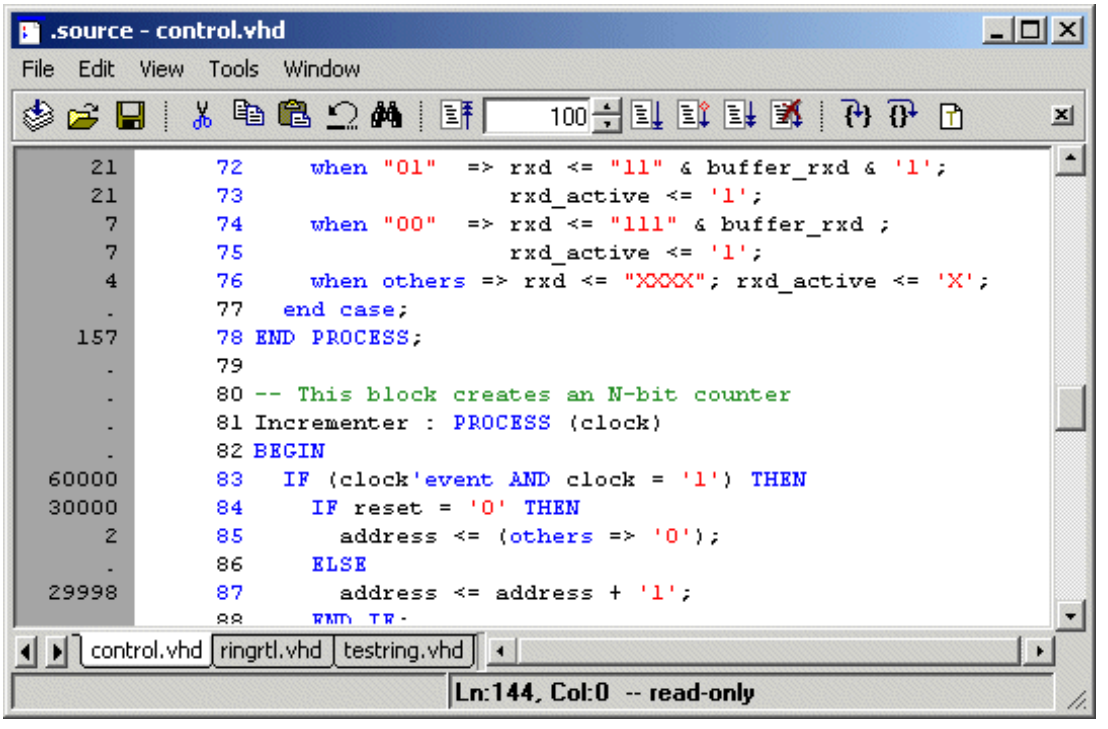
5 Run the simulator for 3 milliseconds as before.

```
run 3 ms
```

Note that now both *testring.vhd* and *control.vhd* are above 90% and therefore shown in green.



6 Click on the *control.vhd* pathname to bring up the Source window. You can see from the values in the first column that the line hits from this run have been added to the ones from the last run. The number of times the clocked processes have been run has doubled.



7 Quit the simulator.

```
quit -f
```

Lesson 8 - Comparing waveforms

The goals for this lesson are:

- Compare two simulations using the Comparison Wizard
- View comparison results and timing difference markers in the Wave window
- Use compare icons to jump to "previous" and "next" difference markers
- View comparison results in the List window
- Set an edge tolerance

Waveform Comparison computes timing differences between test signals and reference signals. In this exercise we're going to run and save the mixedHDL simulation, edit one of the source files, run the simulation again, and finally compare the two runs.

The general procedure for comparing waveforms has four main steps:

1 Selecting the simulations or datasets to compare

2 Specifying the signals or regions to compare

3 Running the comparison

4 Viewing the comparison results

Note: The Waveform Comparison feature is available as an add-on to the PE version. Contact Model Technology sales for more information.

Creating the reference dataset

We'll start by running a simulation and saving it to a dataset. This dataset will become the reference dataset when we set up the comparison.

1. Start by creating a new directory for this exercise. Create the directory and copy all of the files from *\<install_dir>\modeltech\examples\mixedHDL* to the new directory.

   Make sure the new directory is the current directory. Do this by invoking ModelSim from the new directory or by selecting the **File > Change Directory** command from the ModelSim Main window.

2. At the ModelSim prompt in the Transcript pane, run the compare.do DO file.

   ```
   do compare.do
   ```

   This DO file does the following:

   - Creates and maps the work library
   - Compiles the Verilog and VHDL files
   - Runs the simulation and saves the results to a dataset named "gold.wlf"

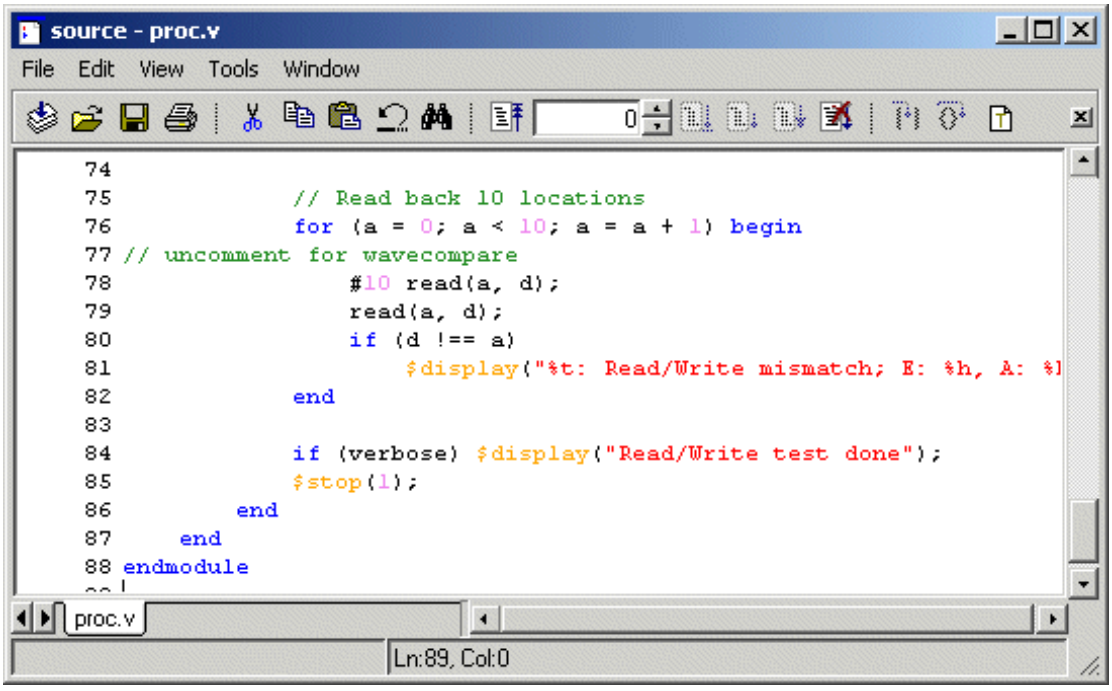
   Feel free to open the DO file and take a look at its contents.

Editing a source file and re-running the simulation

In the last step, we ran the default mixed HDL simulation and saved it to the *gold.wlf* dataset. Now we'll edit one of the source files and re-run the simulation.

1. Edit the *proc.v* file by opening it in the Source window. Make sure the **Edit > read only** flag isn't selected.

2. Scroll down and un-comment the read cycle on line 78. Your source file should look like the following:



3. Save the file in the Source window.

(MENU: File > Save)

4. Re-compile the *proc.v* file.

(PROMPT: vlog proc.v)

(Main MENU: Compile > Compile)

5 Load the top design unit.

(PROMPT: vsim work.top)

(MENU: Simulate > Simulate)

6 Add the waves to the Wave window and run the simulation.

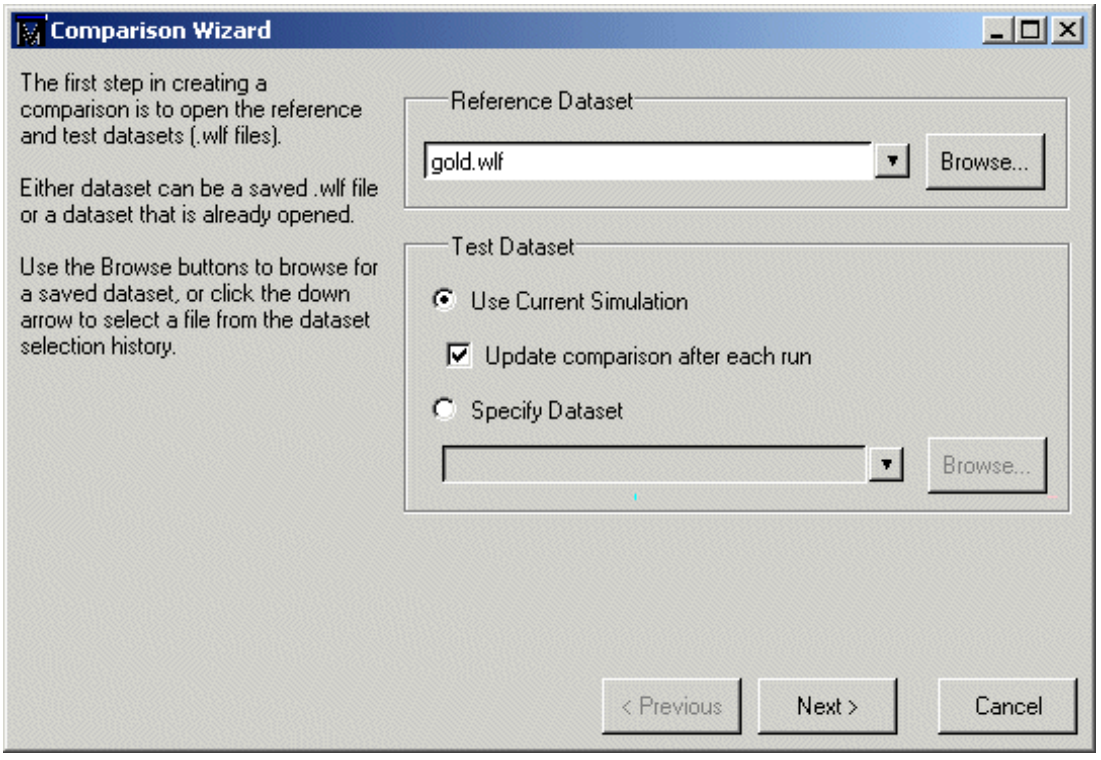
```
add wave *
run -all
```

Comparing the simulation runs

ModelSim includes a Comparison Wizard that walks you through the steps of setting up a waveform comparison. You can also do it manually with menu or command line commands.

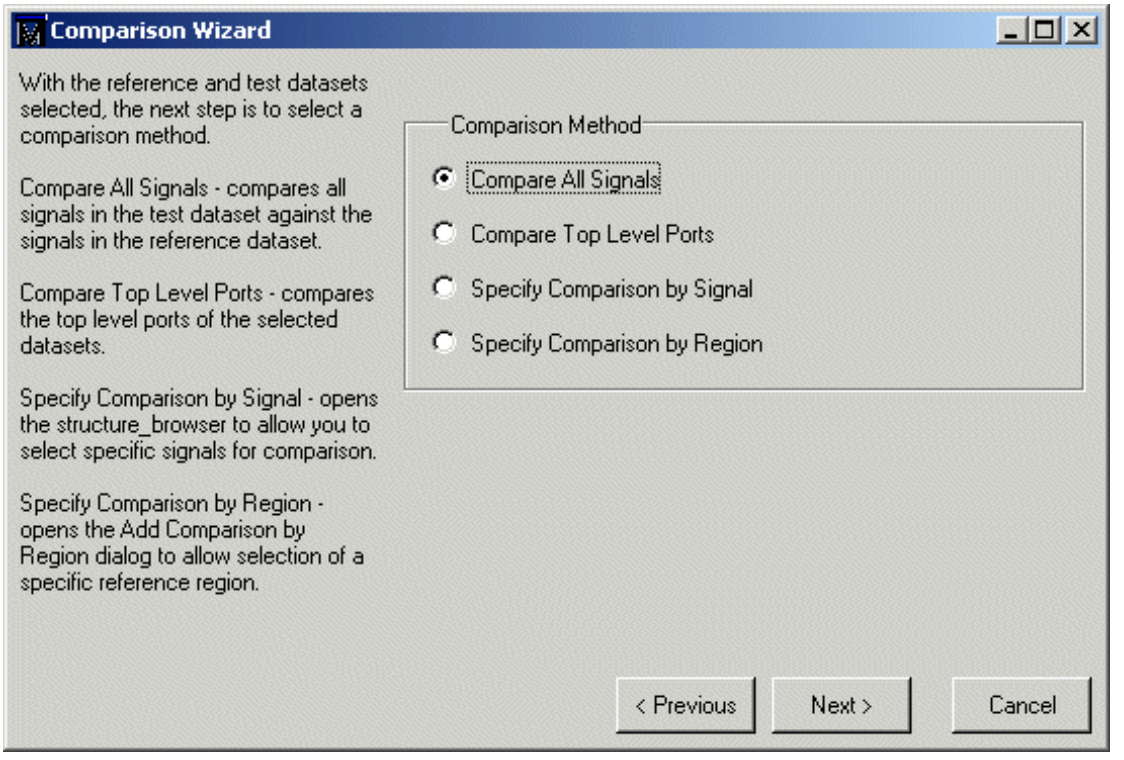
1. Select **Tools > Waveform Compare > Comparison Wizard** from the Wave or Main window.

2. Click the browse button and select *gold.wlf* as the Reference Dataset. Recall that this dataset is from the first simulation run prior to adding the 10 time unit delay.



Leave the Test Dataset set to **Use Current Simulation**, and then click Next.

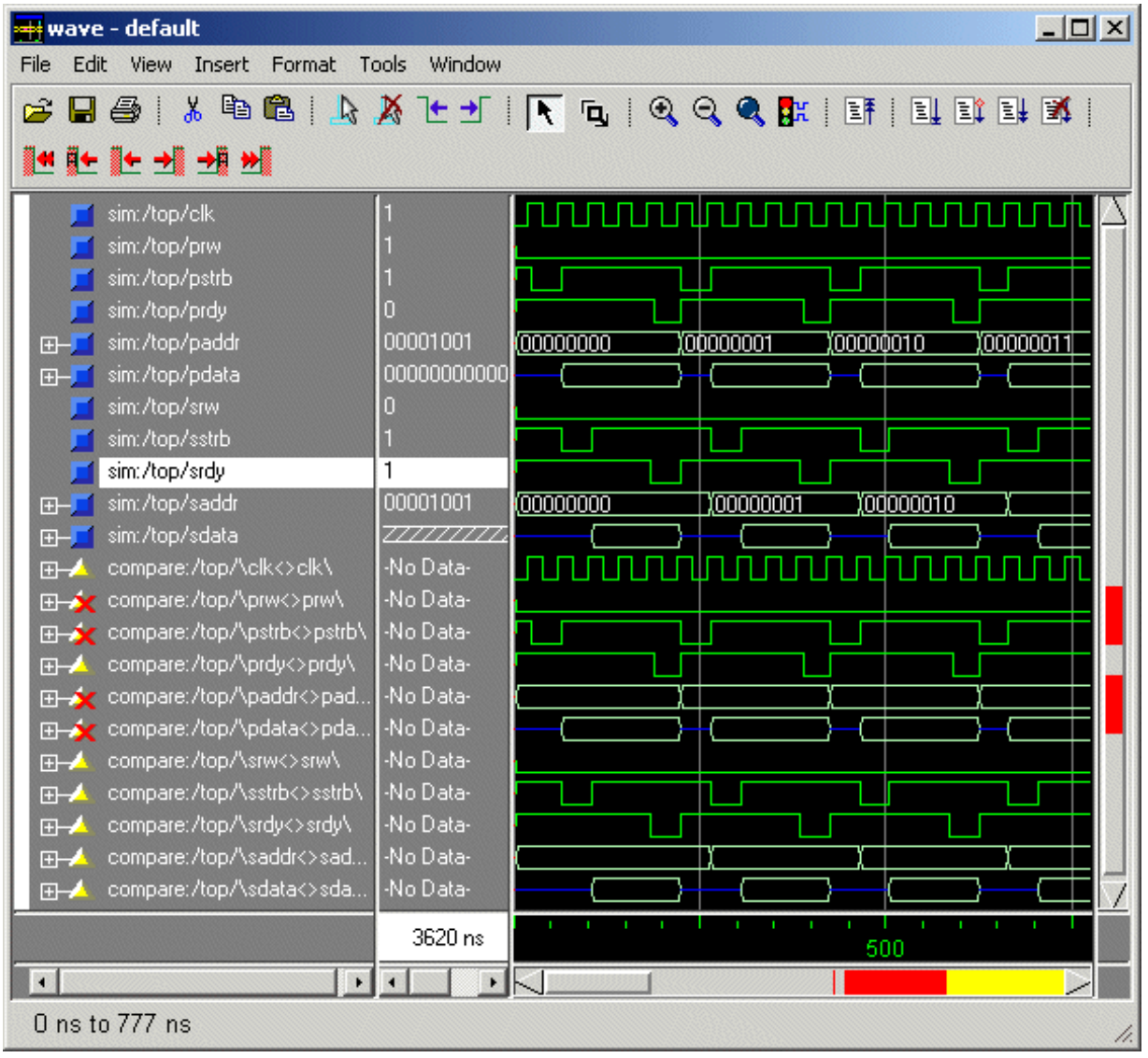
3 Select **Compare All Signals** in the second dialog, and then click Next.



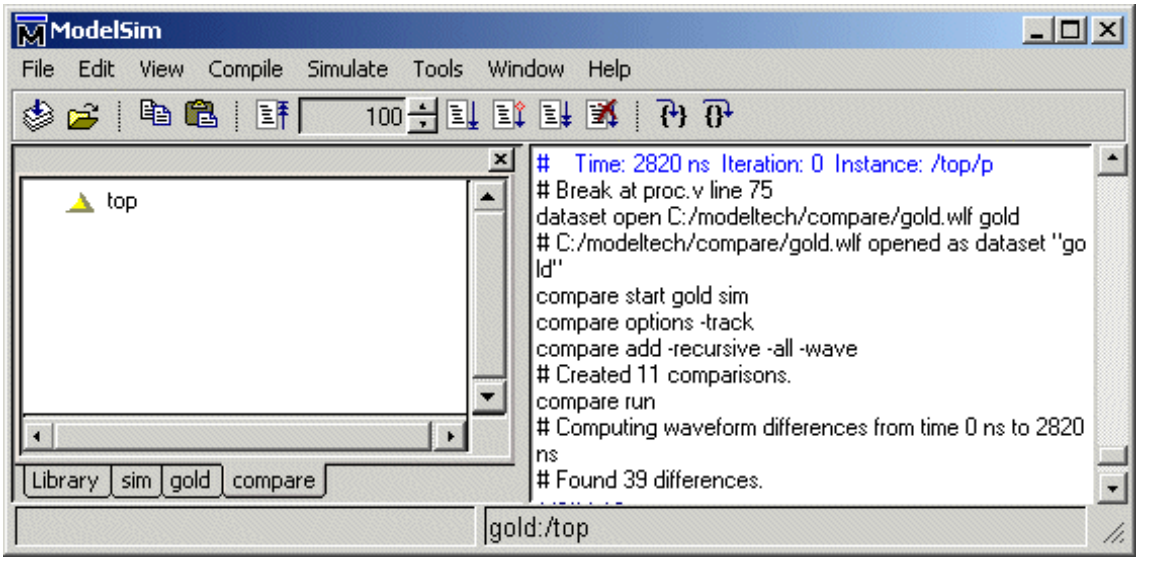
4 In the next three dialogs, click Next, Compute Differences Now, and Finish, respectively.

Viewing and saving the comparison data

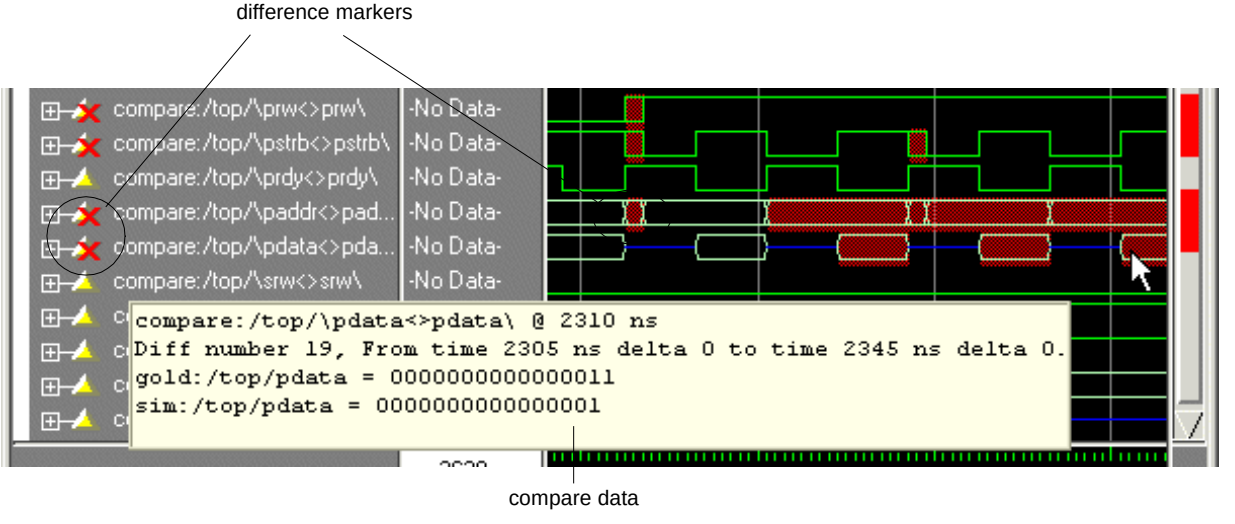
ModelSim performs the comparison and displays the compared signals in the Wave window.



The Compare tab in the Main window shows the region that was compared, and the transcript area shows the number of differences found between the timing of the Reference and Test datasets.



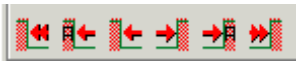
In the Wave window, a signal that contains timing differences between the two simulations is denoted by a red X over its yellow triangle. Red difference markers in the waveform display area show the location of the timing differences on the waveforms, as do the red lines in the horizontal scrollbar at the bottom of the window.



Hover your mouse pointer over a difference marker to display a popup containing data about that timing difference. Also note that when you place a waveform cursor over a difference, the values column displays the text "diff."

Compare icons

The Wave window includes six waveform comparison icons that let you quickly jump between differences. From left to right, the icons do the following: find first difference, find previous annotated difference, find previous difference, find next difference, find next annotated difference, find last difference. Use these icons to move the selected cursor.



The next and previous buttons cycle through differences on all signals. To view differences for just the selected signal, use <tab> and <shift> - <tab>.

Saving the comparison

You can save the comparison for later viewing, either in a text file or in files that can be reloaded into ModelSim.

To save the difference information to a text file, select **Tools > Waveform Compare > Differences > Write Report**.

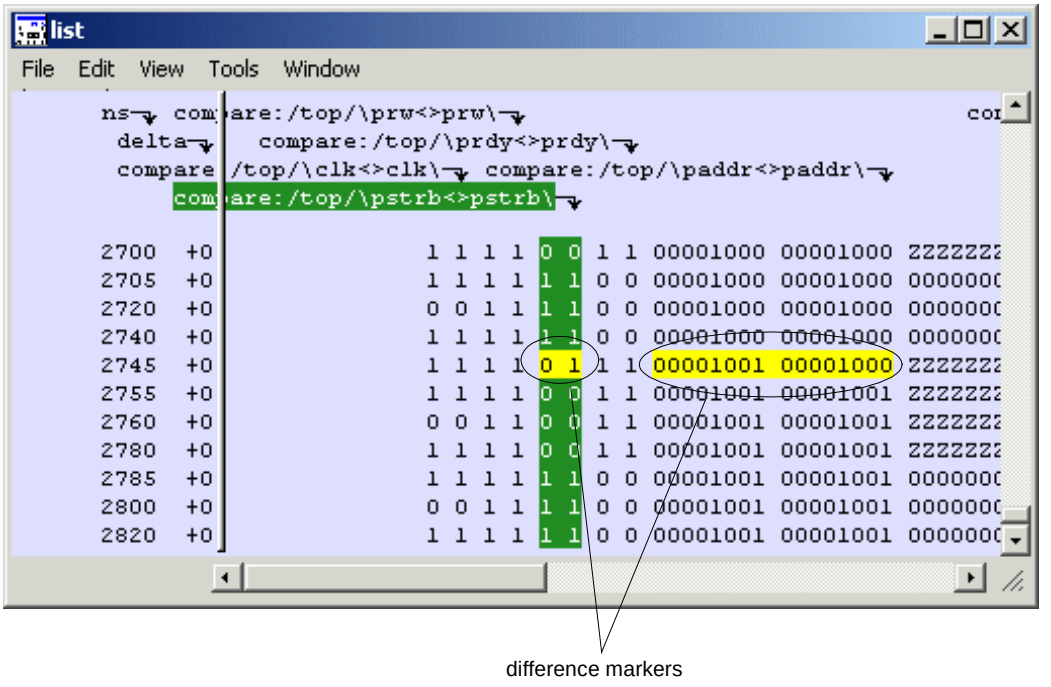
To save the comparison so it can be reloaded into ModelSim, you must save two files. Select **Tools > Waveform Compare > Differences > Save** to save the computed differences. Next, select **Tools > Waveform Compare > Rules > Save** to save the comparison configuration rules. To reload the comparison later, you would start a comparison and then use the **Tools > Waveform Compare > Reload** command.

Viewing comparison results in the List window

You can also view the results of your waveform comparison in the List window.

1. Select **View** > **List** to open the List window.

2. Drag the region from the Compare tab in the Main window to the List window. This will load the compared signals into the List window. Scroll down the window, and you'll see differences shown in yellow.



Specifying tolerances

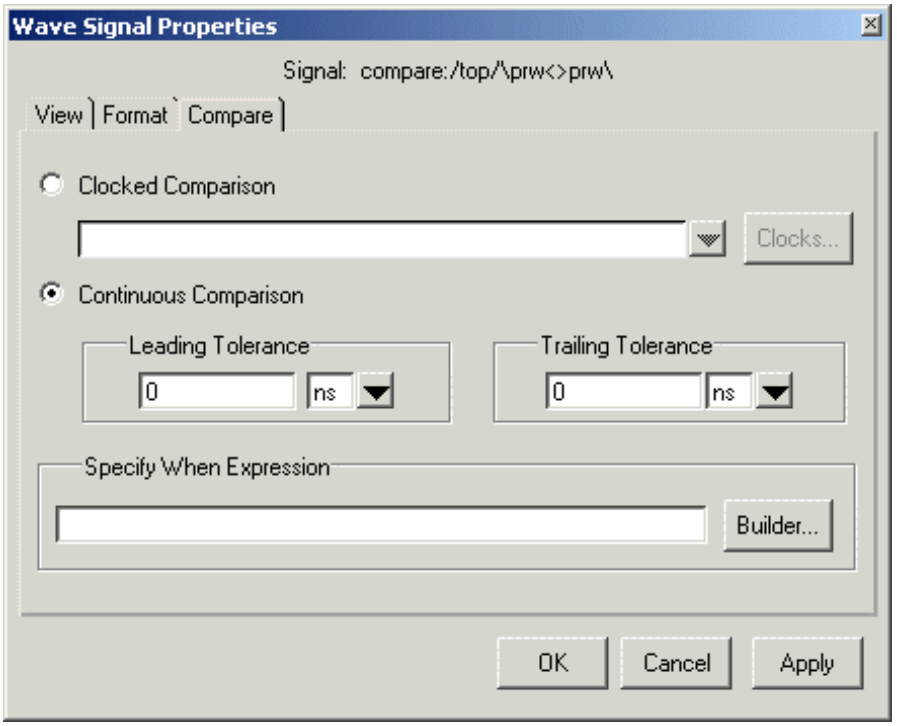
There may be times you want to allow for leading or trailing tolerances in the test dataset signals. You can do this easily by modifying the signal properties of a comparison object in the Wave window.

1 Click the Find Next Difference icon until you can see the differences at 2025 ns.

(KEYBOARD: Tab)

2 Select "compare:/top/\prw<>prw\" in the signals list and then right-click to open the Signal Properties dialog. Select the Compare tab.

(MENU: View > Signal Properties)



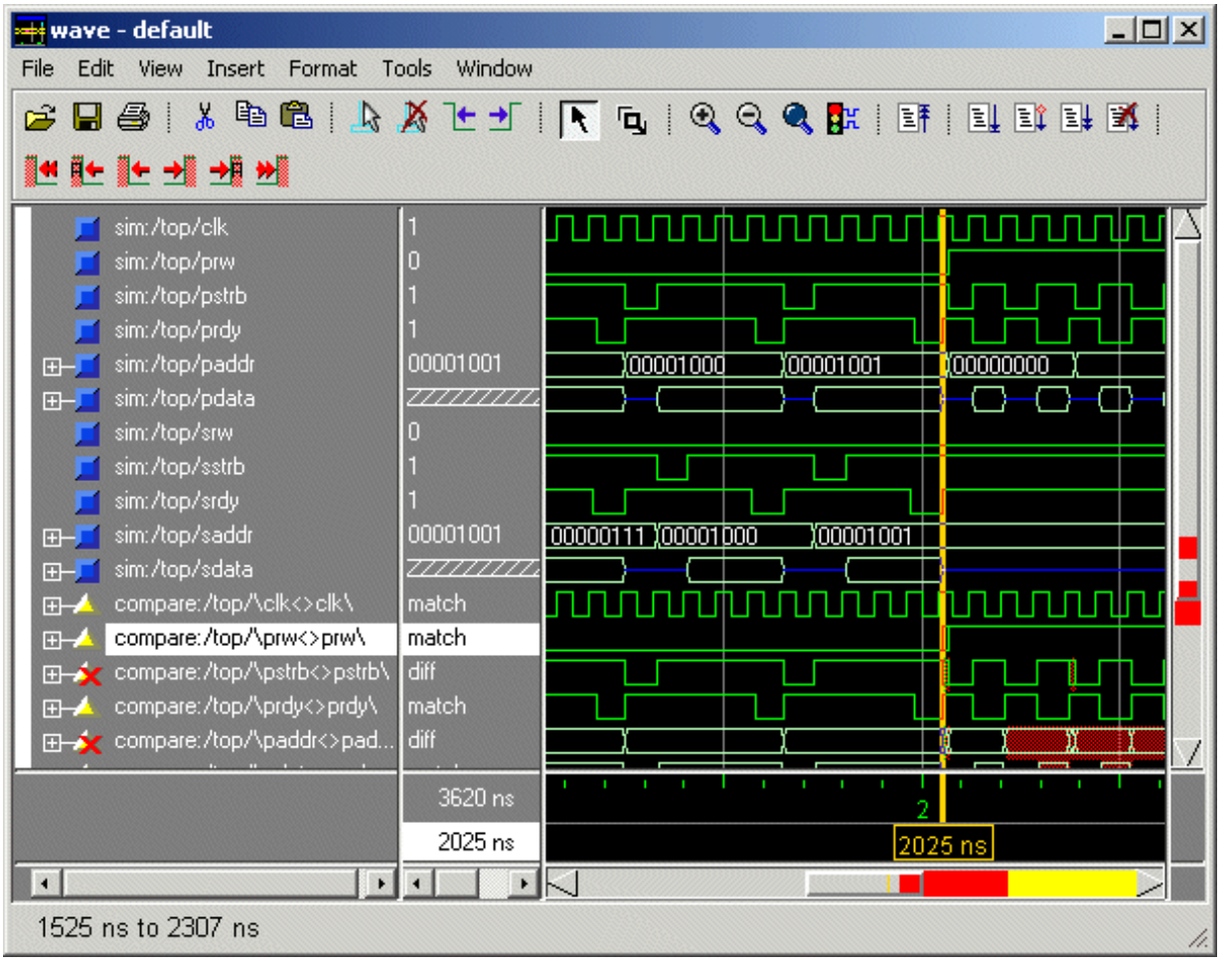
Recall that we delayed the read cycle in *proc.v* by 10 time units. Therefore, if we specify a trailing tolerance of 10 ns, the differences on the comparison object should disappear.

3 Specify 10 ns for the Trailing Tolerance and then click OK.

4 Rerun the comparison.

(MENU: Tools > Waveform Compare > Run Comparison)

5 Notice that the difference markers have disappeared for the /top/prw comparison object.



6 Quit the simulator.

```
quit -f
```

Lesson 9 - Debugging with the Dataflow window

The goals for this lesson are:

- Log signals so you have information necessary for debugging
- Explore the connectivity of your design
- Trace an event
- Trace an X (unknown) value
- Jump to the source of an unknown
- View hierarchy in the Dataflow window
- Zoom and pan the Dataflow window

The Dataflow window allows you trace VHDL signals or Verilog nets and registers through your design. ModelSim versions 5.6 and later include enhanced Dataflow functionality that expands your debugging options.

Note: The enhanced Dataflow window was introduced in version 5.6 and is available as an add-on to the PE product. Contact Model Technology sales for more information.

Compiling and loading the design

We'll start by compiling and loading a mixed design that we'll use for subsequent examples.

1. Create a new working directory, make it the current directory, and then copy the files from *\modeltech\examples\mixedHDL* into it.

2. Use the **vlib** command to create a **work** library in the current directory.

   ```
   vlib work
   ```
   (MENU: File > New > Library)

3. Use the **vmap** command to map the work library to a physical directory. A *modelsim.ini* file will be written into the **work** directory.

   ```
   vmap work work
   ```

4. Compile the Verilog files.

   ```
   vlog cache.v memory.v proc.v
   ```

   
   (MENU: Compile > Compile)

5. Compile the VHDL files.

   ```
   vcom util.vhd set.vhd top.vhd
   ```

   
   (MENU: Compile > Compile)

6. Load the top level of the design.

   ```
   vsim top
   ```

   
   (MENU: Simulate > Simulate)

7. Log all signals in the design so we have all information for debugging.

   ```
   log -r /*
   ```

8. Run the design for 500 ns.

   ```
   run 500 ns
   ```

Exploring connectivity

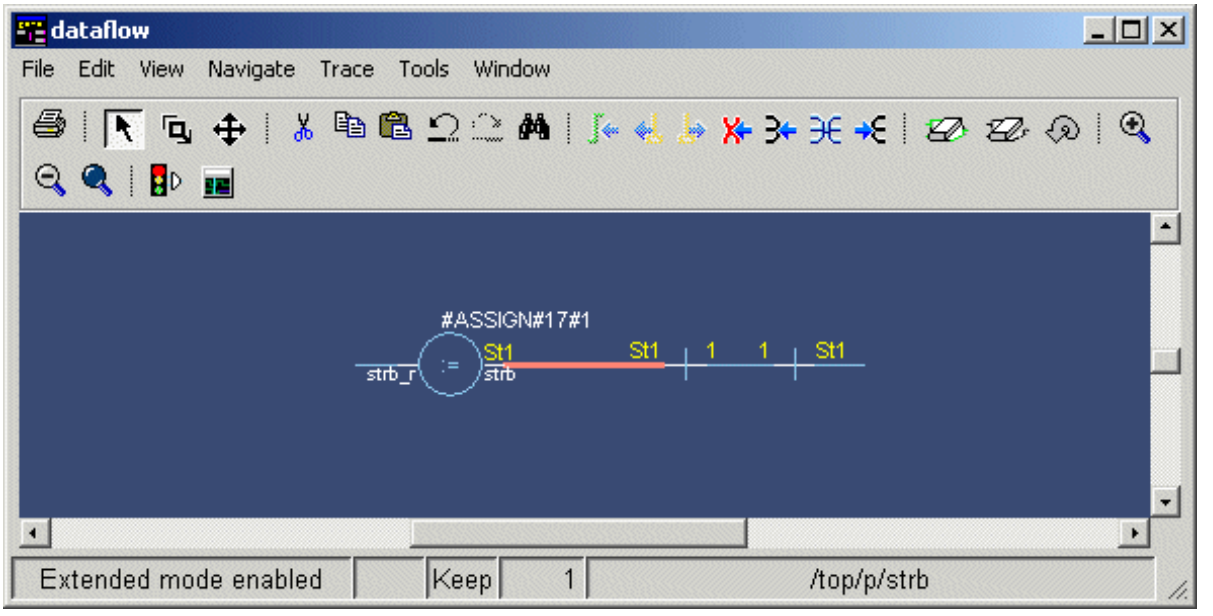
A primary use of the Dataflow window is exploring the "physical" connectivity of your design. You do this by expanding the view from process to process. This allows you to see the drivers/receivers of a particular signal, net, or register.

1. Select *p: proc* in the sim tab of the Main window.

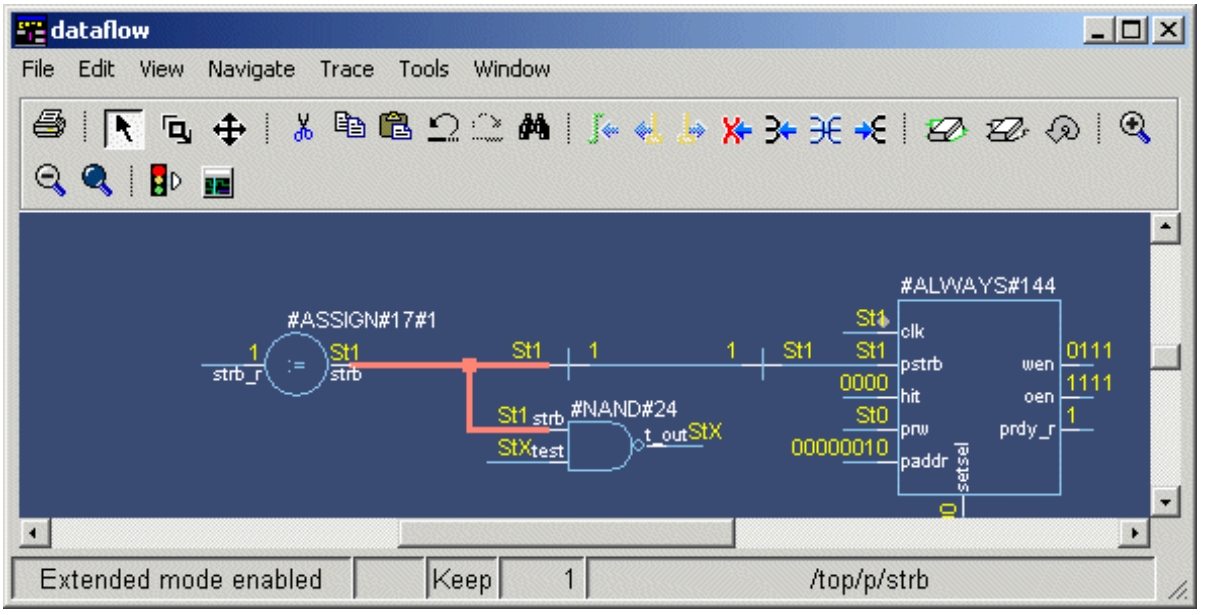
2. Open the Signals and Dataflow windows.

   ```
   view si d
   ```
   (MENU: View > Signals, View > Dataflow)

3. Drag signal *strb* from the Signals window to the Dataflow window.



4 Double click the net that is highlighted in red. The view expands to display the processes that are connected to *strb*.



5 Select signal *test* on process *#AND#24* and expand the view to show its drivers.

(MENU: Navigate > Expand net to drivers)

Notice that after the display expands, the signal line for *strb* is highlighted in green. This highlighting lets you know the path you have traversed in the design.

6 Select signal *oen* on process *#ALWAYS#144*, and expand the view to show its readers.

(MENU: Navigate > Expand net to readers)

7 Continue exploring if you wish. When you are done, clear the Dataflow window before moving on to the next exercise.

(MENU: Edit > Erase all)

Tracing events

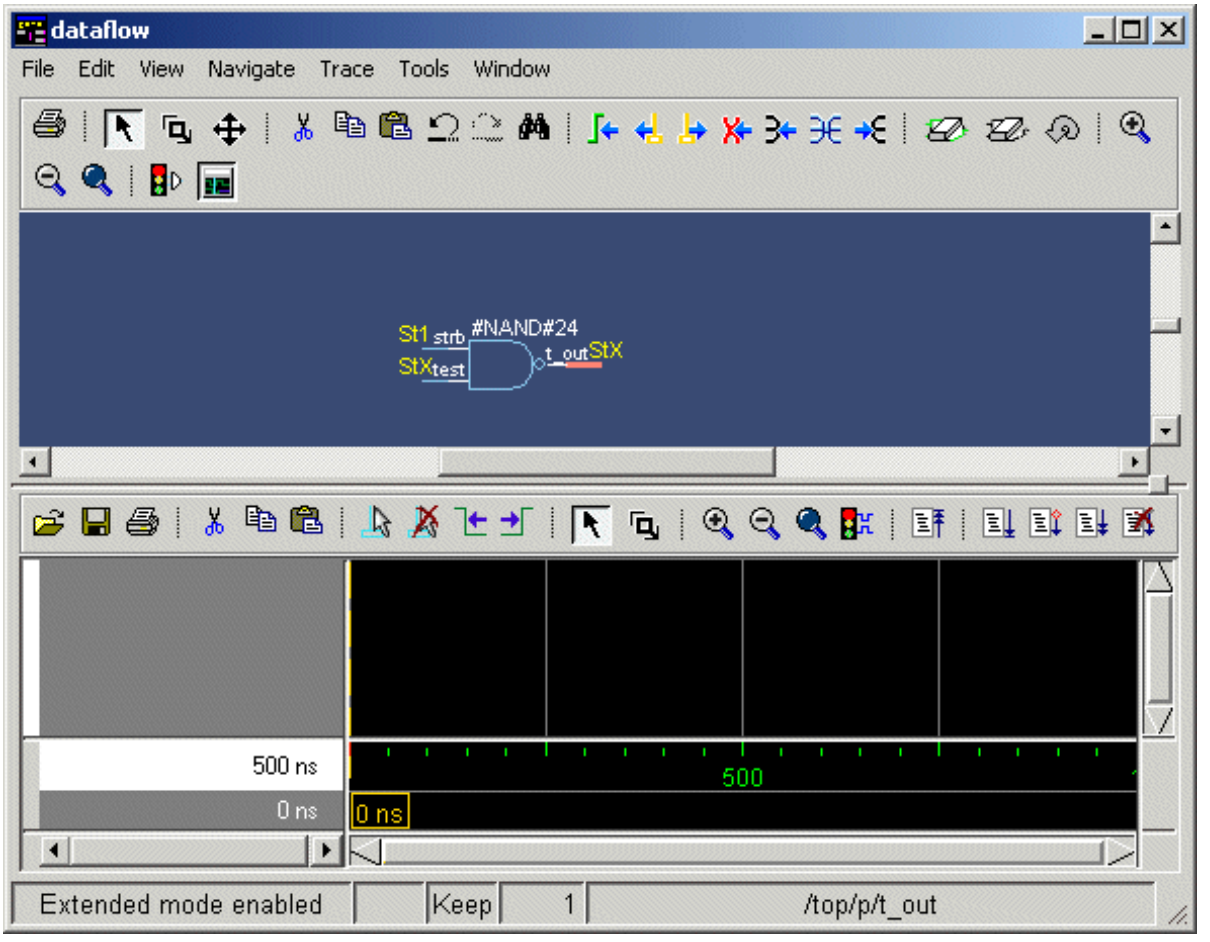
Another useful debugging feature is tracing events that contribute to an unexpected output value. Using the Dataflow window's embedded wave viewer, you can trace backward from a transition to see what process or signal is causing the unexpected output.

1 If you didn't do so in the last exercise, clear the Dataflow window.

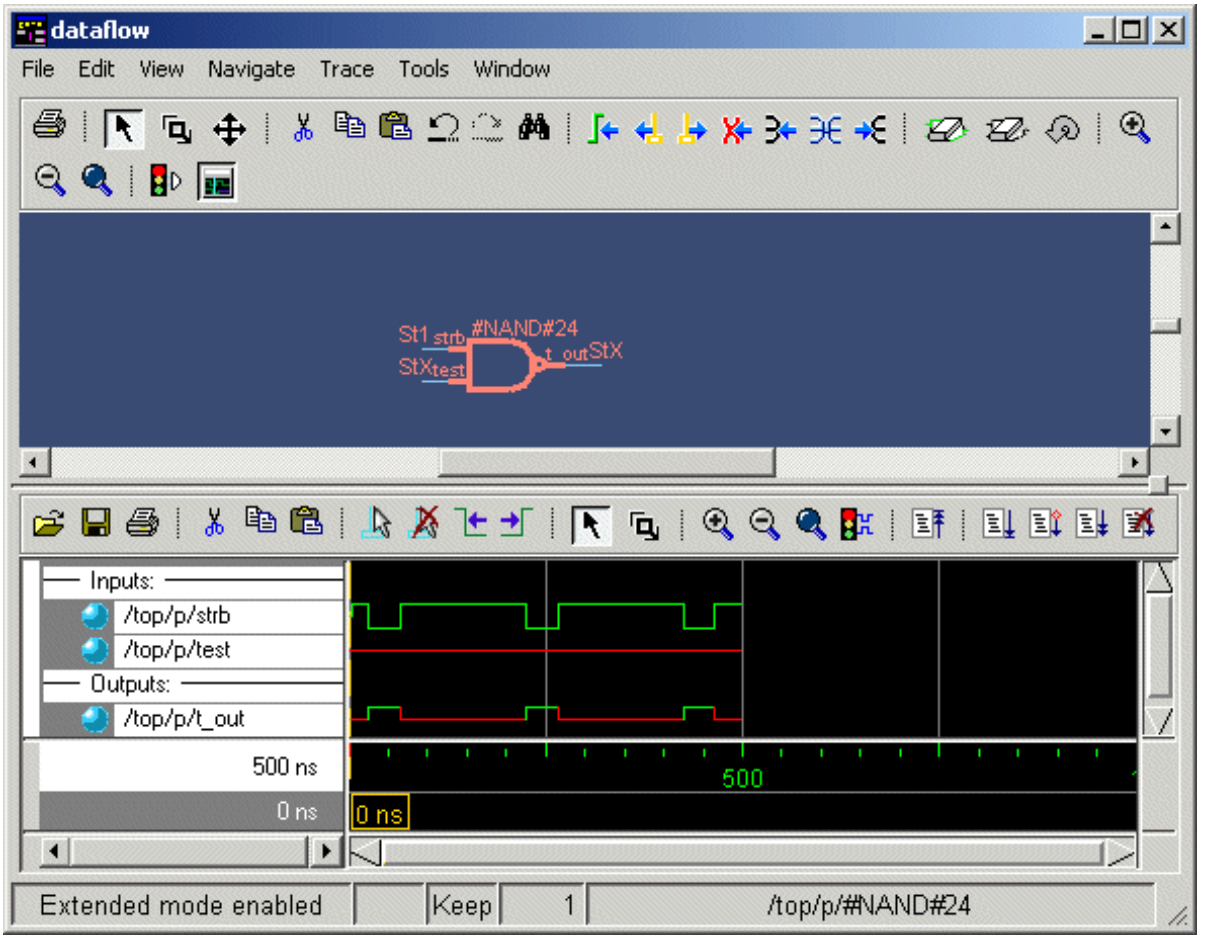
2 Select *p: proc* in the sim tab of the Main window, and then drag signal *t_out* from the Signals window into the Dataflow window.

3 Open the embedded wave viewer and increase the size of the window.

(MENU: View > Show Wave)



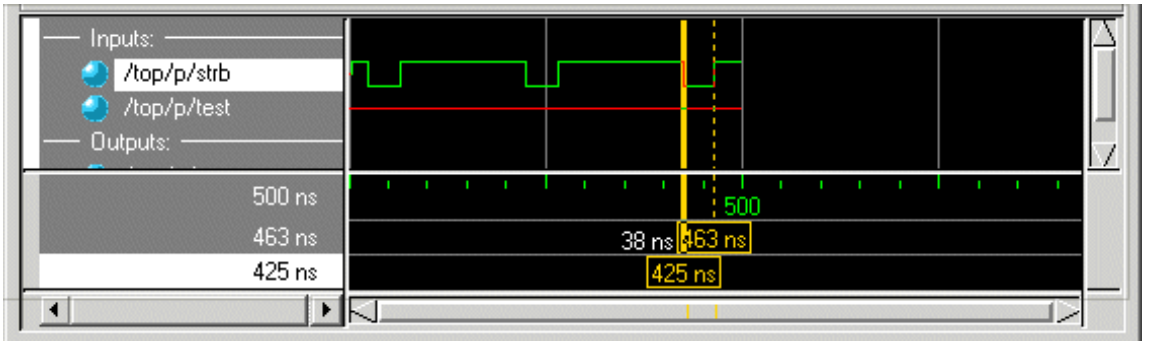
4 Select process *#NAND#24* in the dataflow pane. Notice that all input and output signals of the process are displayed automatically in the wave viewer.



5 Set a time cursor in the wave viewer at the last transition of signal *t_out* (465 ns). See "Making cursor measurements" (T-55) for more information on setting cursors.

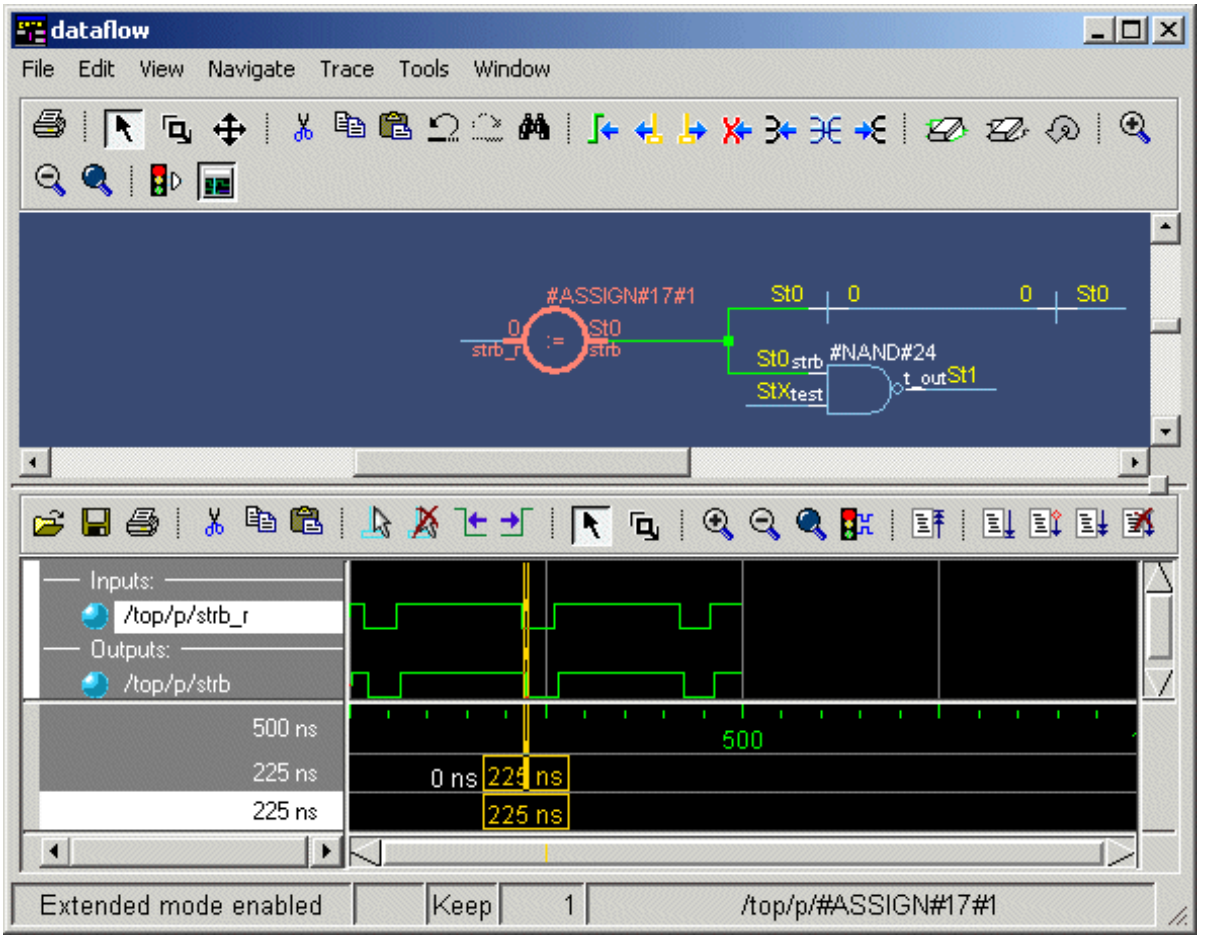
6 To trace to the first contributing event, select **Trace** > **Trace next event**.

A new cursor is added to the wave viewer marking the last event, the transition of the strobe to 0, which caused the output of 0 on *t_out*.



7 Trace the next event two more times and then select **Trace** > **Trace event set**.

The dataflow pane sprouts to the preceding process and shows the input driver of signal *strb*. Notice too that the wave viewer now shows the input and output signals of the newly selected process.



You can continue tracing events through the design in this manner: select **Trace next event** until you get to a transition of interest in the wave viewer, and then select **Trace event set** to update the dataflow pane.

8 Clear the Dataflow window before moving on to the next exercise. Also, close the wave viewer pane.

(MENU: View > Show Wave)

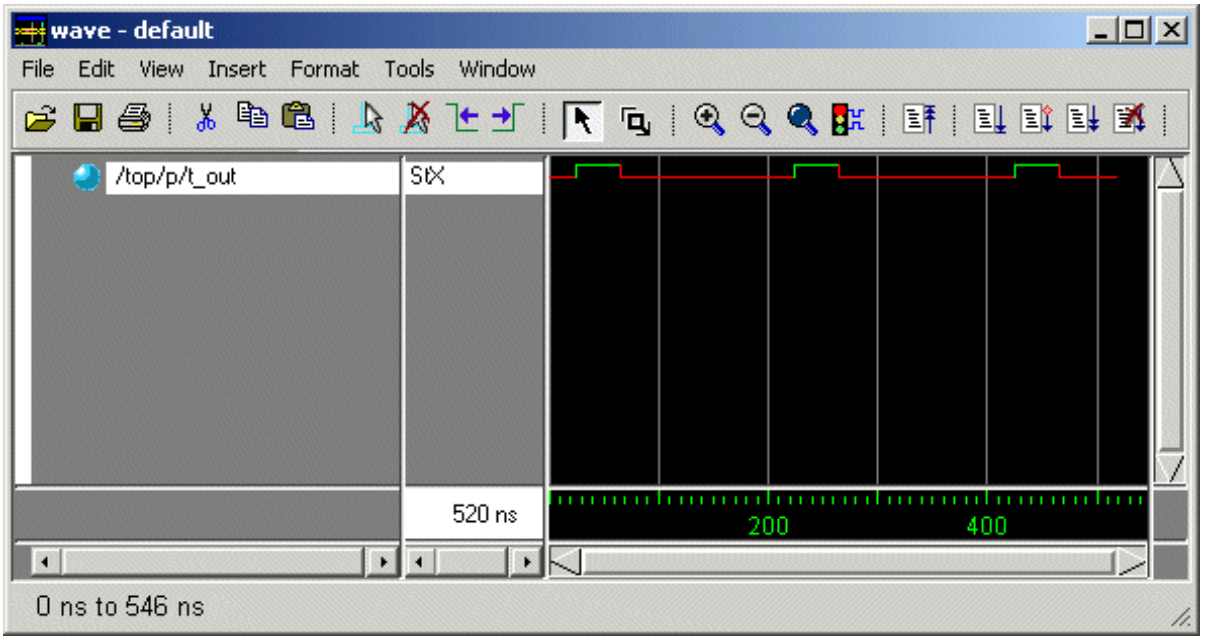
Tracing an 'X' (unknown)

The Dataflow window lets you easily track an unknown value (X) as it propagates through the design. The Dataflow window is linked to the stand-alone Wave window, so you can view signals in the Wave window and then use the Dataflow window to track the source of a problem. As you traverse your design in the Dataflow window, appropriate signals will be added automatically to the Wave window.

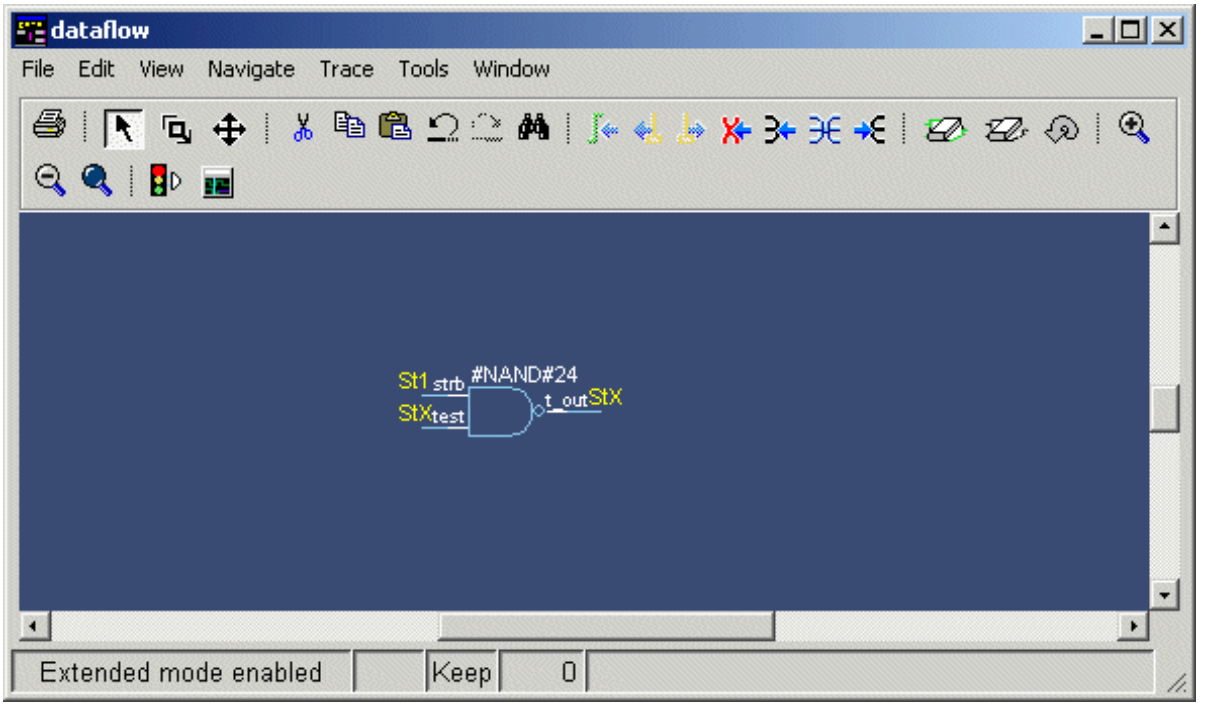
1 Open the Wave window and add a signal.

```
view wave
add wave /top/p/t_out
```
(MENU: View > Wave)
(GUI: Open Signals window and drag signal to Wave window)

Note that *t_out* goes to an unknown state (StX) at time 0 and continues transitioning to StX throughout the run. The red color of the waveform indicates an unknown value.



2 Drag *t_out* from the Wave window to the Dataflow window.



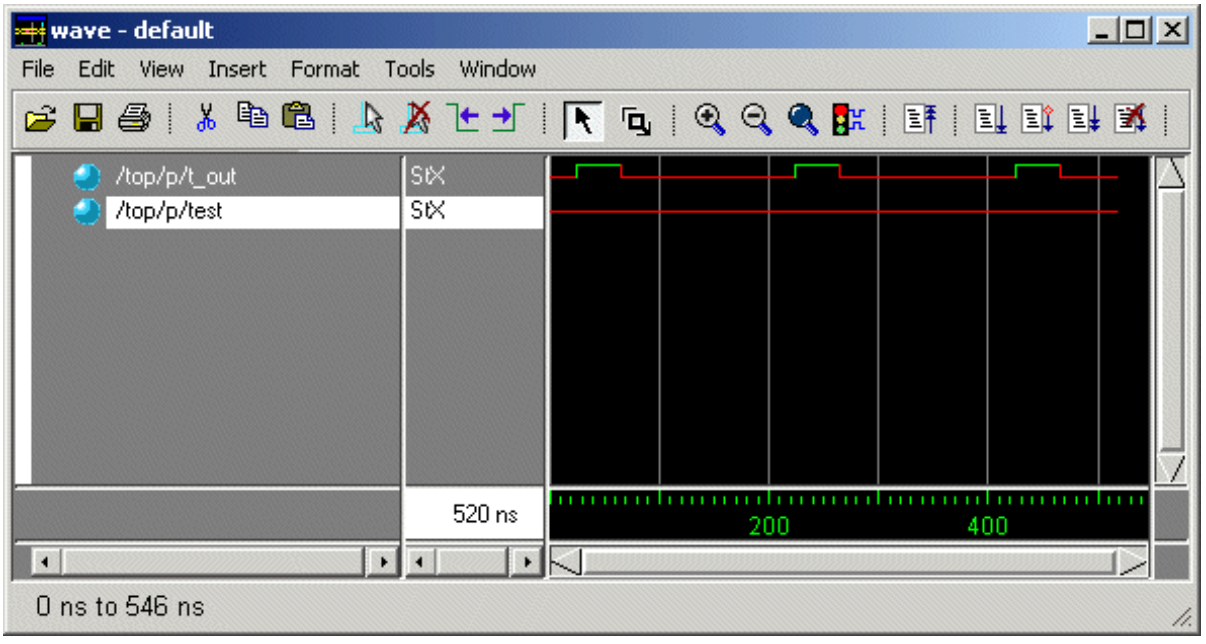
You must click somewhere in the Dataflow window to get the yellow signal values to appear.

As previously mentioned the Wave and Dataflow windows are designed to work together. Try moving the cursor in the Wave window (see "Making cursor measurements" (T-55) for details), and you'll see that the value of *t_out* changes in the Dataflow window. We'll look at other links between the windows as we work through the tutorial.

3 Move the Wave window cursor back to a time when *t_out* is unknown. Then, with *t_out* selected in the Dataflow window, trace the unknown.

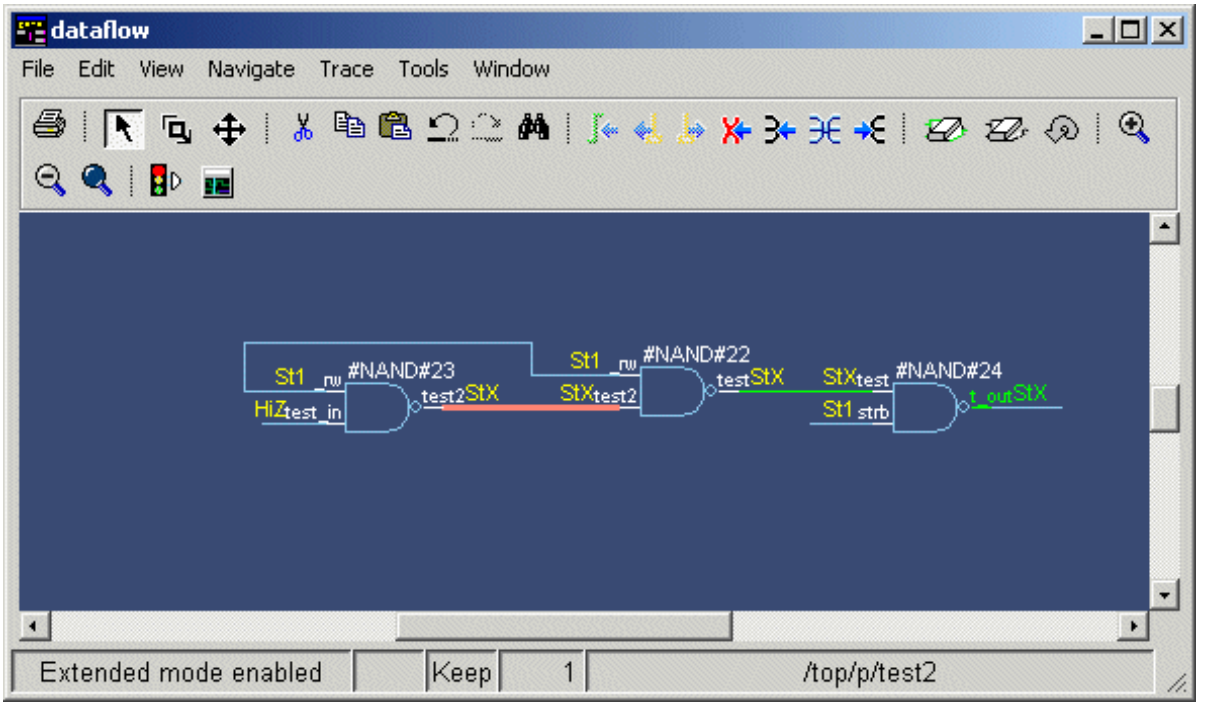
(MENU: Trace > Trace X)

The input signal *test* is selected in the Dataflow window, and it is also added automatically to the Wave window.



4 Continue tracing back to the source of the unknown. Select **Trace** > **Trace X** again. This time signal *test2* is highlighted in the Dataflow window, and it is also added to the Wave window.

5 Select **Trace > Trace X** once more, and you'll discover the source of the unknown. In this case there is a HiZ on input signal *test_in* and a 1 on input signal *_rw*, so output signal *test2* resolves to an 'X'.



6 Clear the Dataflow window.

(MENU: Edit > Erase All)

Jumping to the source of an X

In the last exercise you traced an unknown, from process to process, until you identified the source. You can speed this up by jumping directly to the source in one step.

1. Drag *t_out* from the Wave window to the Dataflow window as you did in the last exercise.
2. Select **Trace > Chase X**.
3. The design expands to show the source of the unknown.
4. Clear the Dataflow window.

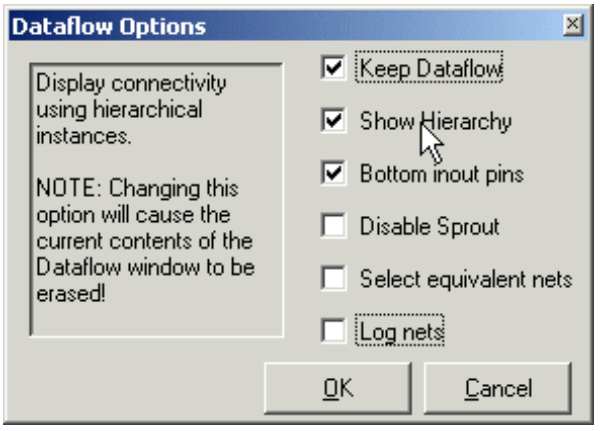
(MENU: Edit > Erase All)

Displaying hierarchy in the Dataflow window

You can display connectivity in the Dataflow window using hierarchical instances. You enable this by modifying the options prior to adding items to the window.

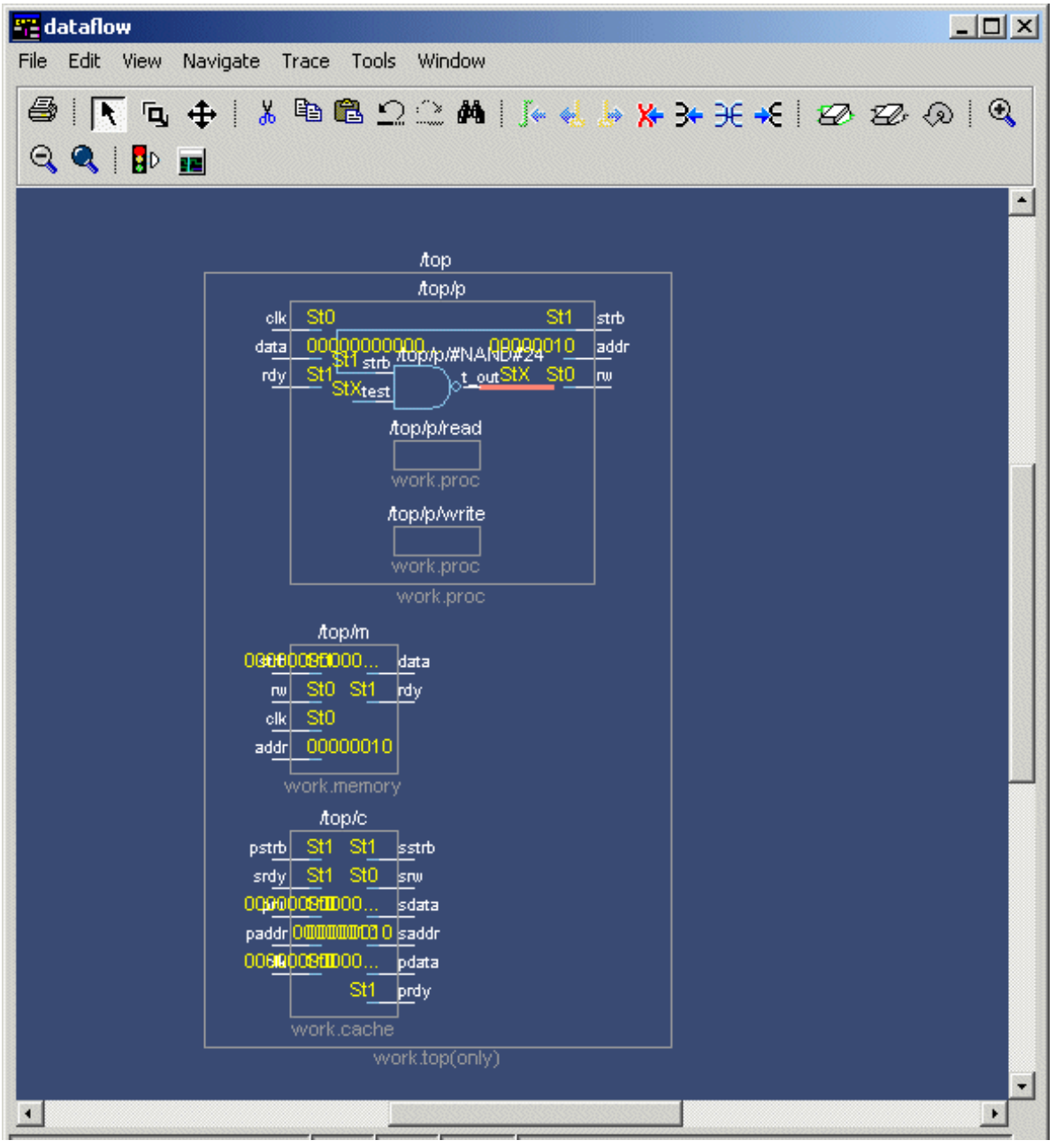
1 Select **Tools > Options** from the Dataflow window menu bar.

2 Check **Show Hierarchy** and then select OK.



3 Add signal *t_out* to the Dataflow window.

```
add dataflow /top/p/t_out
```



Zooming and panning

The Dataflow window offers several tools for zooming and panning the display. After reviewing the options below, try them out on the *cache* module design.

Zooming with toolbar buttons

These zoom buttons are available on the toolbar:

 **Zoom in 2x** zoom in by a factor of two from the current view	 **Zoom out 2x** zoom out by a factor of two from current view
 **Zoom Full** zoom out to view the entire schematic	

Zooming with the mouse

To zoom with the mouse, you can either use the middle mouse button or enter Zoom Mode by selecting **View > Zoom** and then use the left mouse button.

4 zoom options are possible by clicking and dragging in different directions:

- Down-Right: Zoom Area (In)
- Up-Right: Zoom Out (zoom amount is displayed at the mouse cursor)
- Down-Left: Zoom Selected
- Up-Left: Zoom Full

The zoom amount is displayed at the mouse cursor. A zoom operation must be more than 10 pixels to activate.

Panning with the mouse

To pan with the mouse you must enter Pan Mode by selecting **View > Pan**.

Now click and drag with the left mouse button to pan the design.

Lesson 10 - Running a batch-mode simulation

The goals for this lesson are:

- Run a batch-mode VHDL simulation
- Execute a macro (DO) file
- View a saved simulation

Batch-mode allows you to execute several commands that are written in a text file. You create a text file with the list of commands you wish to run, and then specify that file when you start ModelSim. This is particularly useful when you need to run a simulation or a set of commands repeatedly.

Important: Batch-mode simulations must be run from a DOS prompt. Unless directed otherwise, enter all commands in this lesson at a DOS prompt. Additionally, this lesson assumes you have added ModelSim to your PATH. If you did not, you'll need to specify full paths to the tools (i.e., vlib, vmap, vcom, and vsim) that are used in the lesson.

1. To set up for this lesson, create a new directory and copy this file into it:

   ```
   \<install_dir>\modeltech\examples\counter.vhd
   ```

2. Create a new design library (again, enter these commands at a DOS prompt in the new directory you created in step 1.):

   ```
   vlib work
   ```

3. Map the library:

   ```
   vmap work work
   ```

4. Then compile the source file:

   ```
   <install_dir>/<platform>/vcom counter.vhd
   ```

5. You will use a macro file that provides stimulus for the counter. For your convenience, a macro file has been provided with ModelSim. You need to copy this macro file from the installation directory to the current directory:

   ```
   <install_dir>\modeltech\examples\stim.do
   ```

6. Create a batch file using an editor; name it *yourfile*. With the editor, put the following on separate lines in the file:

   ```
   add list -decimal *
   do stim.do
   write list counter.lst
   quit -f
   ```

   and save to the current directory.

7. To run the batch-mode simulation, enter the following at the command prompt:

   ```
   vsim -do yourfile -wlf saved.wlf counter -c
   ```

   This is what you just did in Step 7:

   - invoked the VSIM simulator on a design unit called "counter"
   - instructed the simulator to save the simulation results in a log file named *saved.wlf* by using the **-wlf** switch
   - used the contents of *yourfile* to specify that values are to be listed in decimal, to execute a stimulus file called *stim.do*, and to write the results to a file named *counter.lst*, the default for a design named *counter*

8. Since you saved the simulation results in *saved.wlf*, you can view the simulation results by starting up VSIM with its **-view** switch:

   ```
   vsim -view saved.wlf
   ```

9 Open these windows with the **View** menu in the Main window, or the equivalent command at the ModelSim prompt:

```
view signals list wave
```

Note: If you open the Process or Variables windows they will be empty. You are looking at a saved simulation, not examining one interactively; the logfile saved in *saved.wlf* was used to reconstruct the current windows.

10 Now that you have the windows open, put the signals in them:

```
add wave *
add list *
```

11 Use the available windows to experiment with the saved simulation results and quit when you are ready:

```
quit -f
```

For additional information on the batch and command line modes, please refer to the *ModelSim User's Manual*.

Lesson 11 - Executing commands at load time

The goals for this lesson are:

- Specify the design unit to be simulated on the command line
- Edit the *modelsim.ini* file
- Execute commands at load time with a DO file

Important: Start this lesson from the DOS prompt in the same directory in which you completed *Chapter Lesson 10 - Running a batch-mode simulation*.

1 For this lesson, you will use a macro (DO) file that executes whenever you load a design. For convenience, a startup file has been provided with the ModelSim program. You need to copy this DO file from the installation directory to your current directory:

```
\<install_dir>\modeltech\examples\startup.do
```

2 Next, you will edit the *modelsim.ini* file in the *\modeltech* directory (or the *modelsim.ini* file in your current directory if one exists) to point at this file. To do this, open *<install_dir>\modeltech\modelsim.ini* using a text editor and uncomment the following line (by deleting the leading ;) in the [vsim] section of the file:

```
Startup = do startup.do
```

Then save *modelsim.ini*.

Note: The *modelsim.ini* file must be write-enabled for this change to take place. Using MS Explorer, right-click on *\<install_dir>\modeltech\modelsim.ini*, then click Properties. In the dialog box, uncheck the Read-only box and click OK. (You can also copy the file to your current directory.)

3 Take a look at the DO file. It uses the predefined variable **$entity** to do different things when loading different designs.

4 Start the simulator and specify the top-level design unit to be simulated by entering the following command at the DOS prompt:

```
vsim counter
```

Notice that the simulator loads the design unit without displaying the Load Design dialog box. This is handy if you are simulating the same design unit over and over. Also notice that all the windows are open. This is because the **view *** command is included in the startup macro.

5 If you plan to continue with the following practice sessions, keep ModelSim running. If you would like to quit the simulator, enter the following command at the VSIM prompt:

```
quit -f
```

6 You won't need the *startup.do* file for any other examples, so use your text editor to comment out the "Startup" line in *modelsim.ini*.

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